

## Model Name: GA-Z87-HD3

1.02

SHEET

TITLE

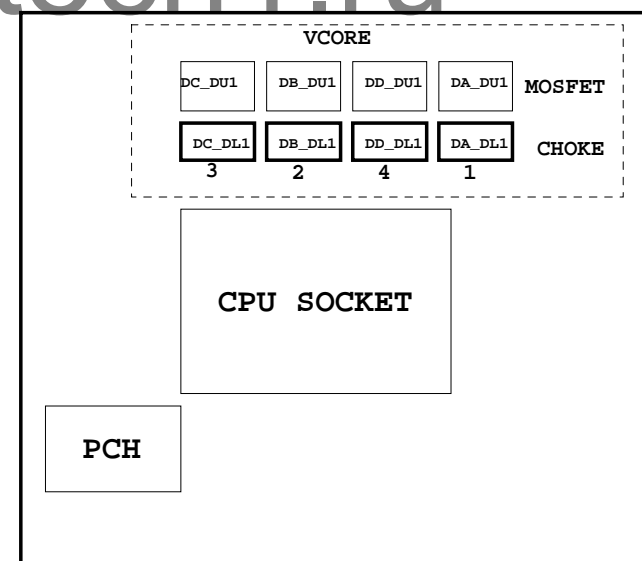
01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1150-A
05	CPU_LGA1150-B
06	CPU_LGA1150-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	PCH_FDI,DMI,USB,PCIE
10	PCH_RGB,CLK BUFFER
11	PCH_HOST,SATA,PCI
12	PCH_GPIO,CTRL,AUDIO
13	PCH_PWR,GND
14	PCI EXPRESS*16 SLOT
15	PCIEX1*2 , PCIEX4 SLOT
16	ITE8892 PCI BRIDGE
17	PCI SLOT 1&2
18	I/O ITE8728
19	COM, -PROHOT, R_USB
20	Dual BIOS / LPT
21	ALC892 CODEC
22	REAR AUDIO JACK
23	VCORE_ ISL95820_1
24	VCORE_ ISL95820_2
25	DDR15V / M3 POWER
26	NCP3933 OVER VOLTAGE
27	DISCRETE POWER

SHEET

TITLE

28	F_PANEL , F_USB2.0/3.0
29	ATX POWER, CLOCK GEN
30	HWM , KB/MS , FAN CTRL
31	Realtek 8111F-VL
32	DVI
33	HDMI
34	TABLE LIST
35	
36	
37	
38	
39	
40	

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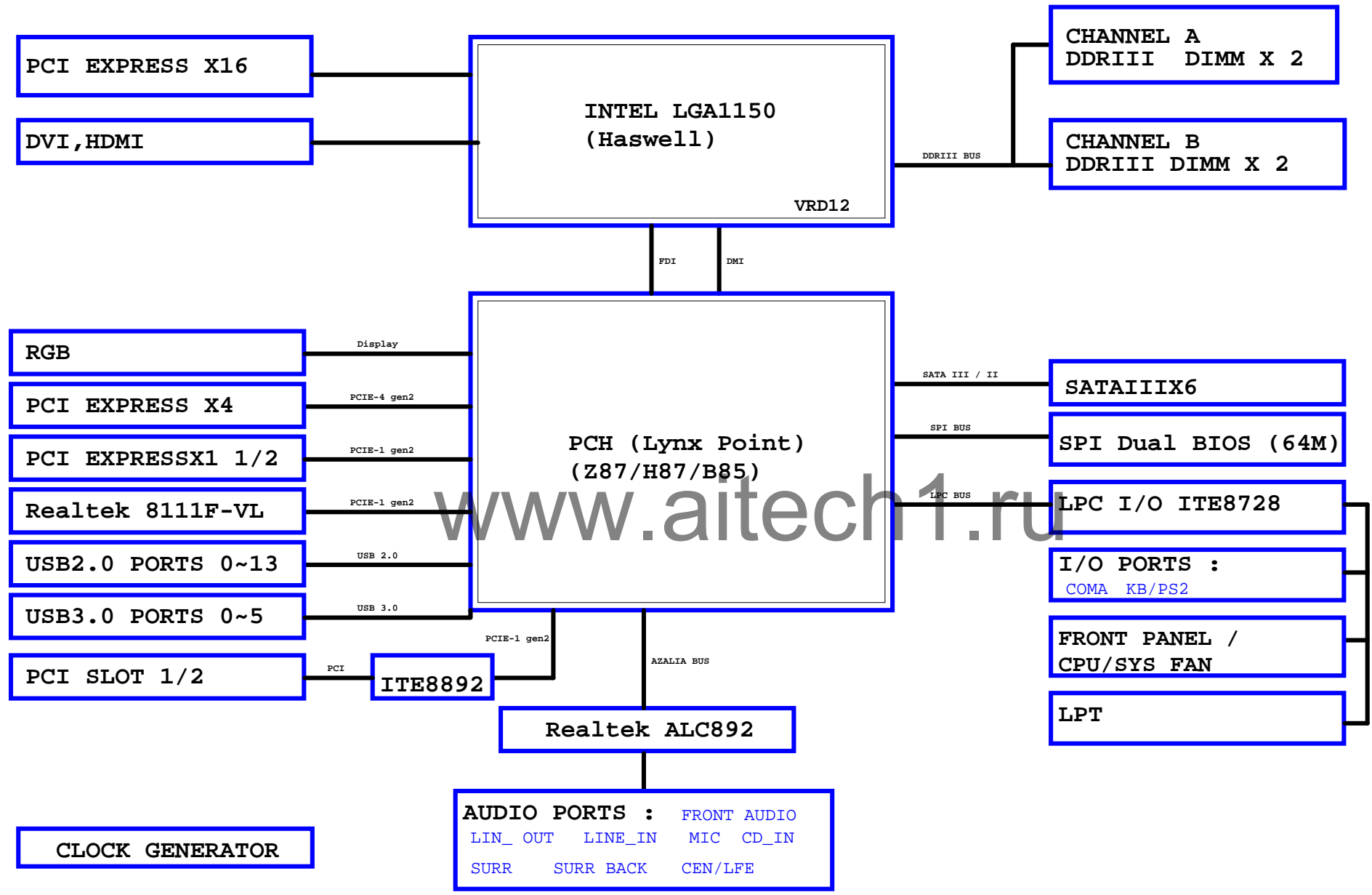


Gigabyte Technology			
Title Cover Sheet			
Size Custom	Document Number	GA-Z87-HD3	Rev 1.02
Date: Friday, March 22, 2013	Sheet 1	of 34	

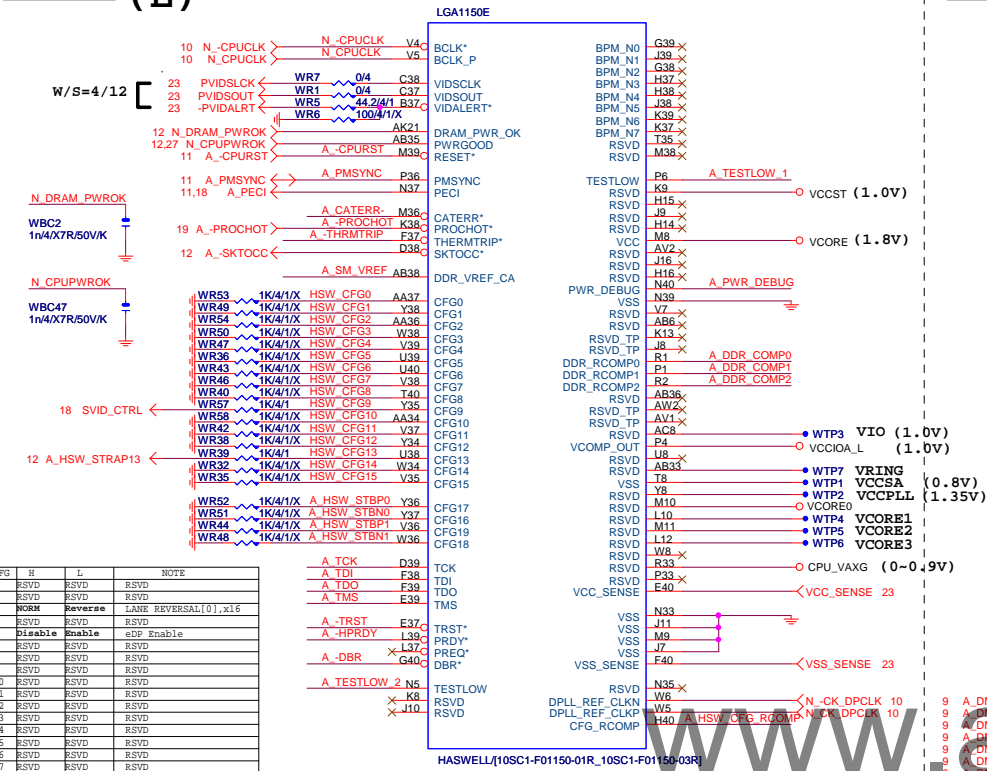
## Component value change history

[illegible][illegible]

BLOCK DIAGRAM



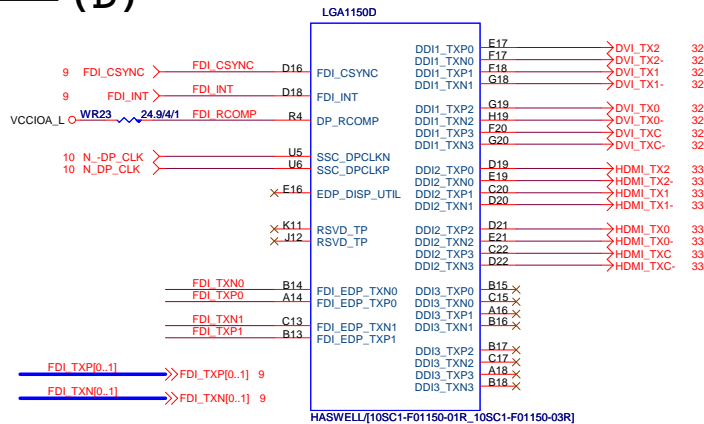
**LGA1150 (E)**



CFG6	CFG5	PCIE CONFIG
1	1	1x16 , Default
1	0	2x8
0	1	RSVD
0	0	X8, X4, X4

G 0-17 all internal PULL-UP

**LGA1150 (D)**



FDI:4/4/4//15(breakout min 4/4/4//8)  
Impedance=85 +- 15%

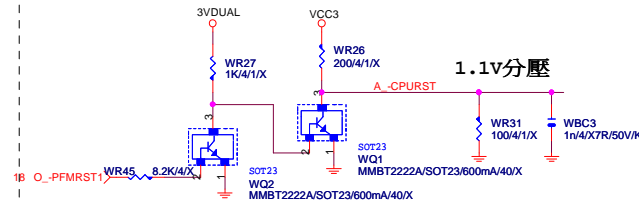
DP/HDMI 4/4/4//20 FDI 4/4/4/12

Impedance=85 +- 15%

LGA1155 (C)



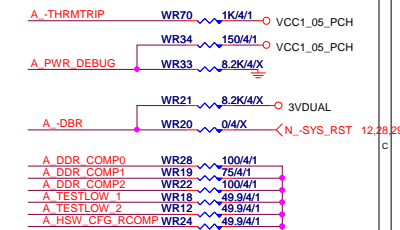
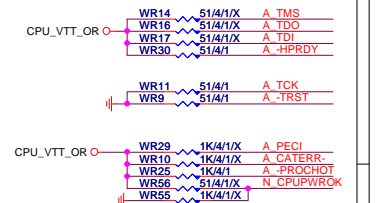
-CPURST



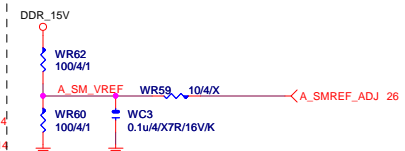
## CPU SVID



## CPU PU/PD



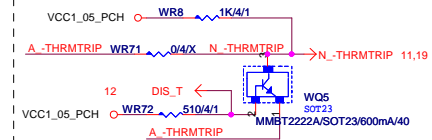
SM REF
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```

| THRMTRIP DISABLE FOR Z87 OVERCLOCK

```

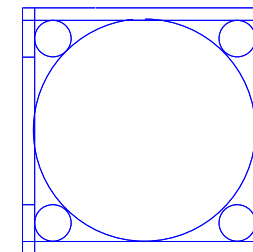




## LGA1150A

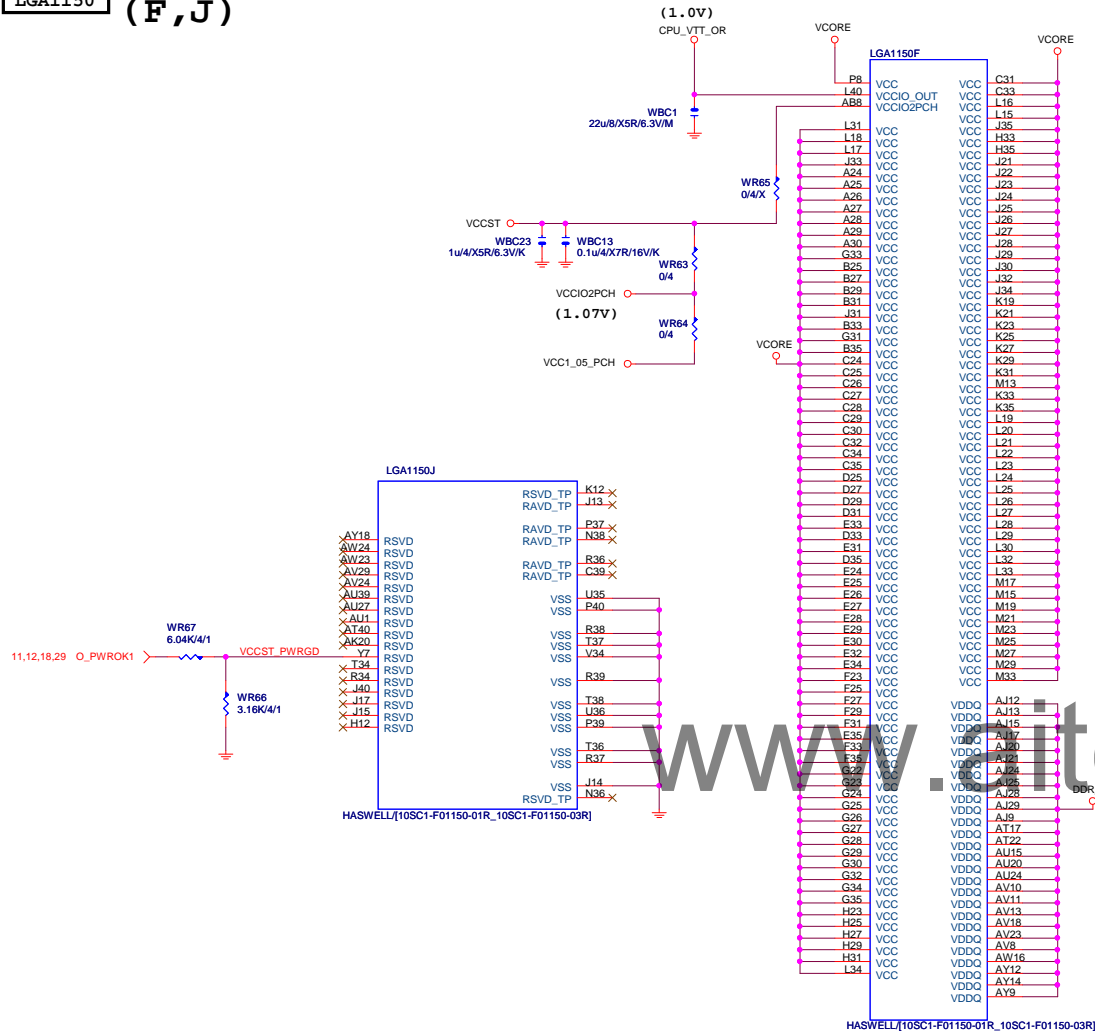
HASWELL/I10SC1-F01150-01R I10SC1-F01150-03R

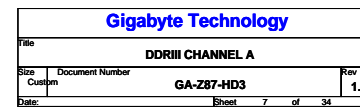
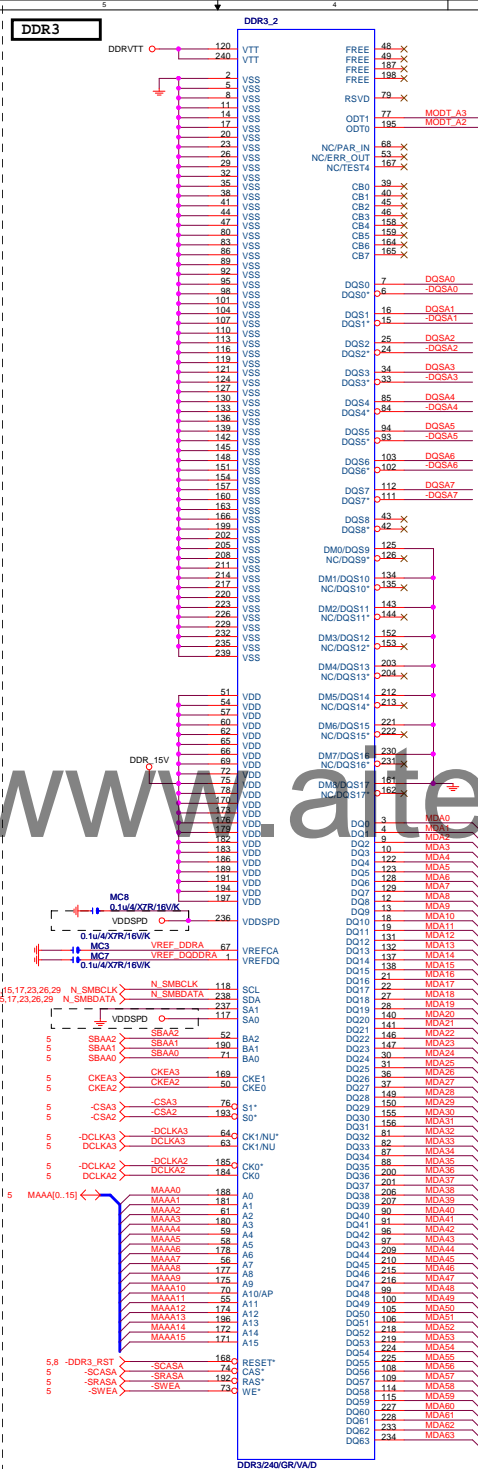
## LGA1150B

HASWELL/10SC1-F01150-01R 10SC1-F01150-03RLGA1150  
ILM\_BP/1156/CSP

7 MODT\_A[0..3] ↔ MODT\_A[0..3]  
 8 MODT\_B[0..3] ↔ MODT\_B[0..3]  
 7 MDA[0..63] ↔ MDA[0..63]  
 8 MDB[0..63] ↔ MDB[0..63]  
 7 DQSA[0..7] ↔ DQSA[0..7]  
 7 -DQSA[0..7] ↔ -DQSA[0..7]  
 7 MAAA[0..15] ↔ MAAA[0..15]  
 8 MAAB[0..15] ↔ MAAB[0..15]  
 8 DQSB[0..7] ↔ DQSB[0..7]  
 8 -DQSB[0..7] ↔ -DQSB[0..7]

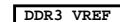
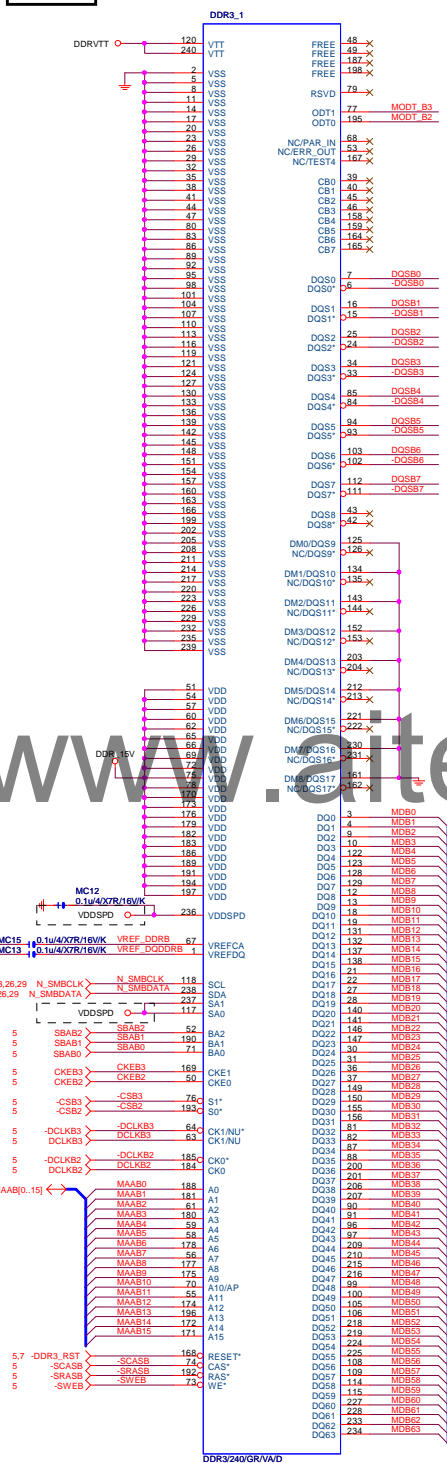
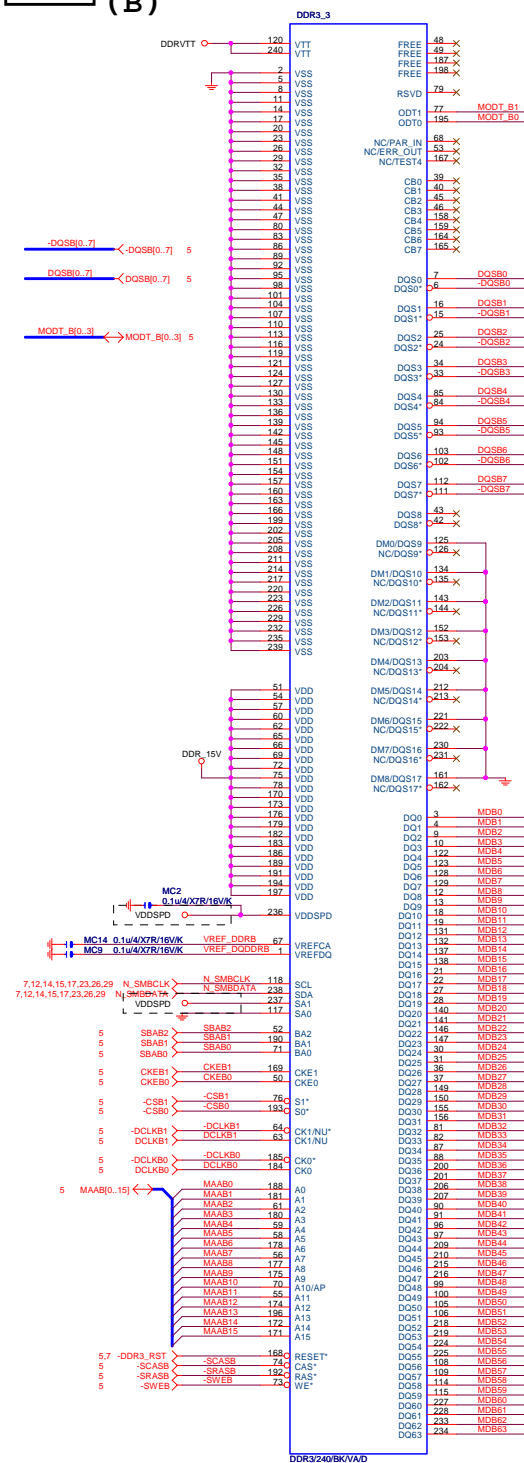
# LGA1150 (F,J)







(B)



DDR3 1066,1333,1600MHZ BANDWIDTH

DDR3 1066MHZ

DDR3 single channel bandwidth=533x2x8Byte=8.5GB/s

DDR3 dual channel bandwidth=533x2x2x8Byte=17GB/s

```
| DDR3 1333MHZ
```

```
DDR3 clock=667MHZ
```

```
DDR3 single channel bandwidth=10.6GB/s
```

DDR3 dual channel bandwidth=21GB/s

DDR3 1600MHZ

```
DDR3 clock=800MHZ
```

```
DDR3 single channel bandwidth=12.8GB/s
```

```
DDR3 dual channel bandwidth=25.6GB/s
```

COUPON



CPU

## DIMM

## DIMM

## DIMM

## DIMM

CHA

CHB

## Gigabyte Technology

Title				DDRIII CHANNEL B			
Size	Document Number						Rev
Custom	GA-Z87-HD3						1.0
Date:				Sheet	8	of	34

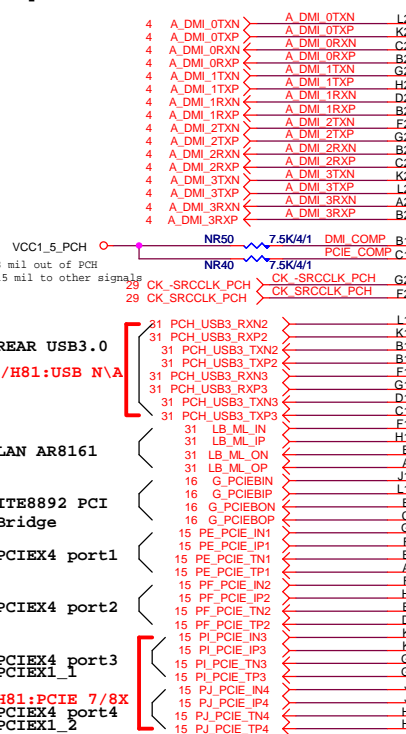
GA-Z87-HD3

Rev
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Date:	Sheet	8	of	3
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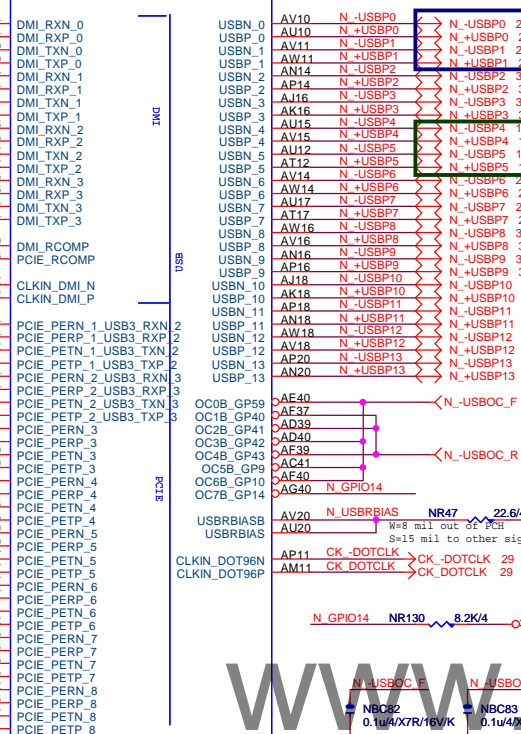
DMI:12/4/4/4/12(breakout min 8/4/4/4/8)  
Impedance=85 +- 17.5%

DMI:12/4/4/4/12(breakout min 8/4/4/4/8)  
Impedance=85 +- 17.5%



放靠近 Device & PCI-E Slot

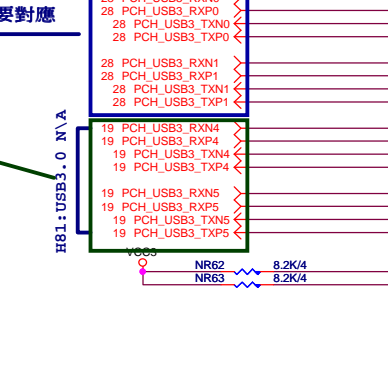
USB2.0 : 12/5/7/5/12 (breakout min 8/4/4/4/8)  
PCHB Impedance=85 +/- 15%



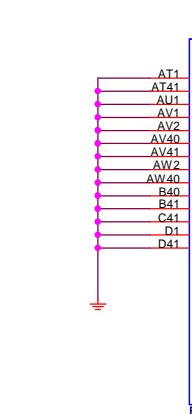
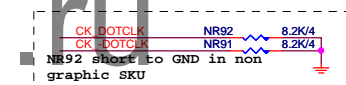
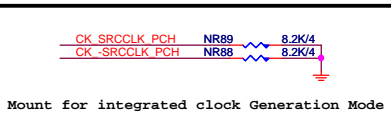
PCH PCIE ,DMI 4/4/4//15 Impedance=85 +- 15%

```
usb2.0 5/7/5//12
usb3.0 5/7/5//20      Impedance=85 +/- 15%
```

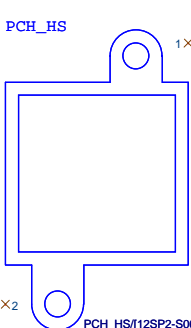
28 PCH\_USB3\_RXN0 >



USB3.0:20/5/7/5/20 (breakout mir  
8/4/4/4/8) ; ONLY 3 VIAS  
Impedance=85 +- 17.5%  
Back Panel < 10000 MILS  
Front Panel < 6000 MILS



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PCH\_HS/12SP2-S06012-01R\_12SP2-S06012-02R\_12SP2-S06012-03R

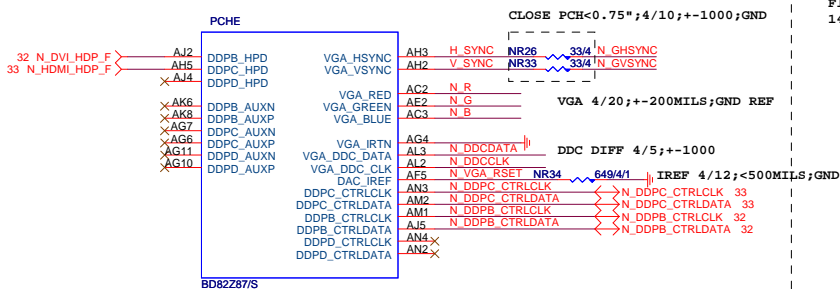
---

```
OC[3:0]# for Device 29 (ports 0-7)
OC[7:4]# for Device 26 (ports 8-13)
```

USB OC#	Configure
OC0#	USB0,1
OC1#	USB2,3
OC2#	USB4,5
OC3#	USB6,7
OC4#	USB8,9
OC5#	USB10,11
OC6#	USB12,13
OC7#	Not Use

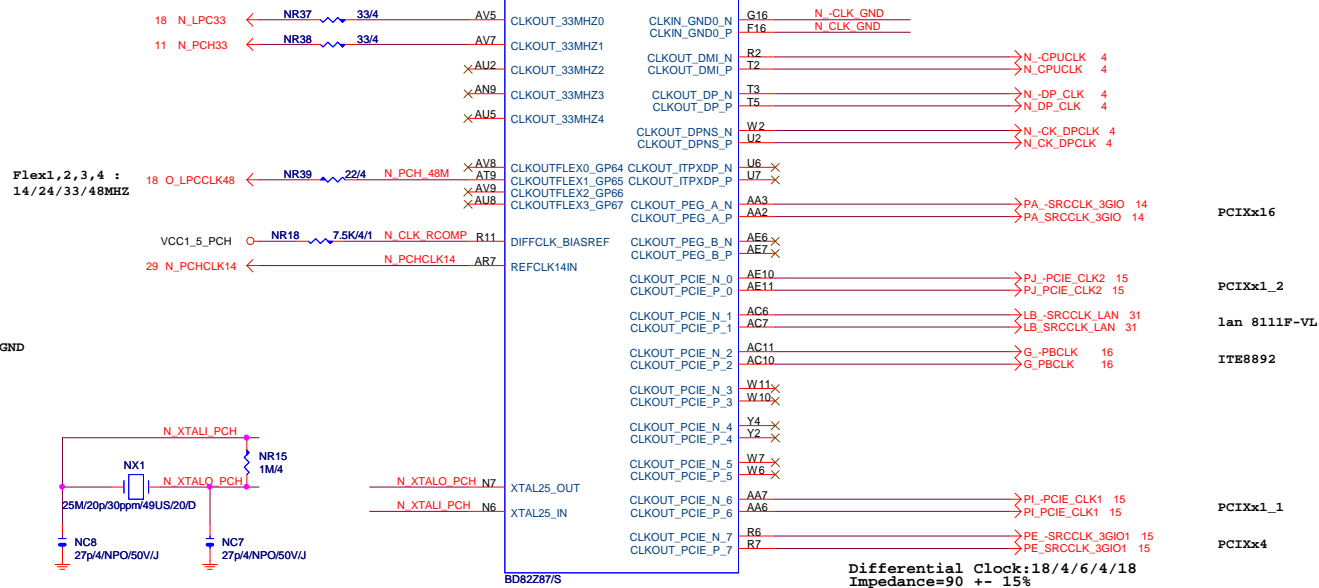


**PCH (E)**

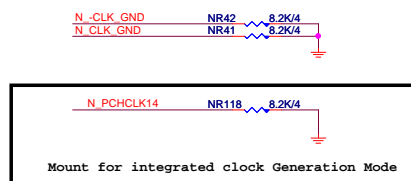


VGA_DISABLE
R,G,B NC OR GND
IRTN / IREF GND
VGA_HSYNC, VGA_VSYNC, DDC_CLK, DDC_DATA NC
POWER_VCCADAC(AF2), VCCADACBG(AE1) GND

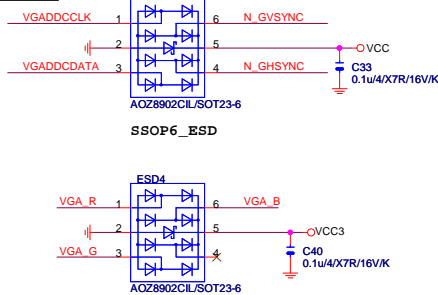
**PCH (G)**



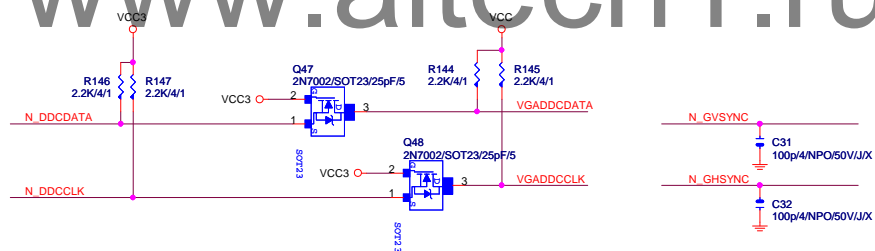
PCH CLK PD
------------



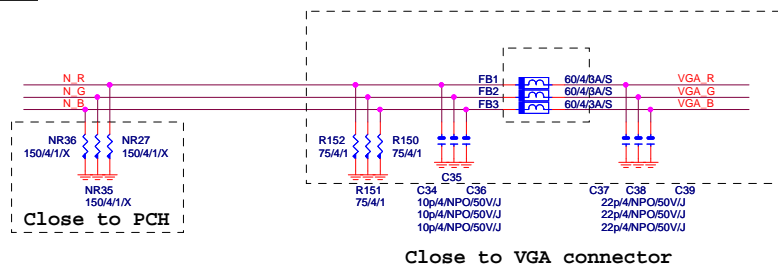
## VGA ESD



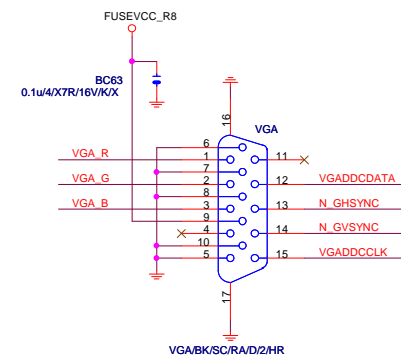
## VGA DDC



## VGA DDC

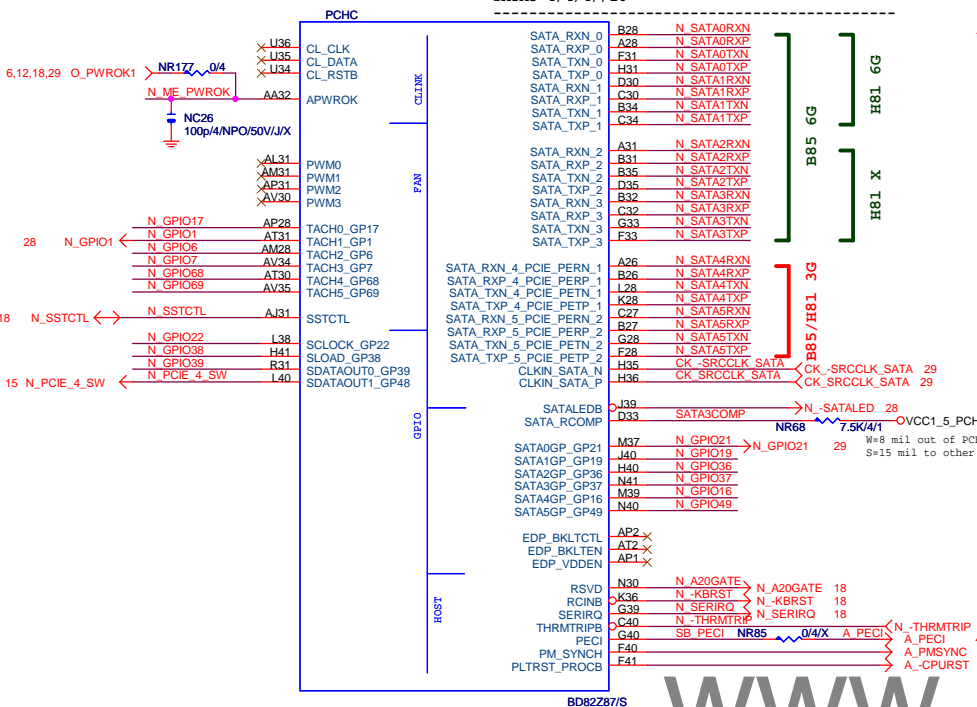


## VGA CONNECTOR

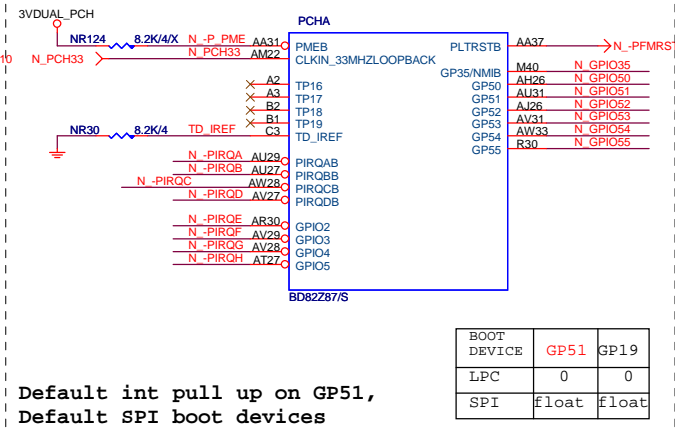


PCH (C)

SATA3 : 20/4/4/20 (breakout min 8/4/4/4/8)  
Impedance=85 +- 17.5%  
SATA2 4/4/4//15  
SATA3 4/4/4//20



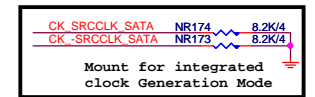
PCH (A)



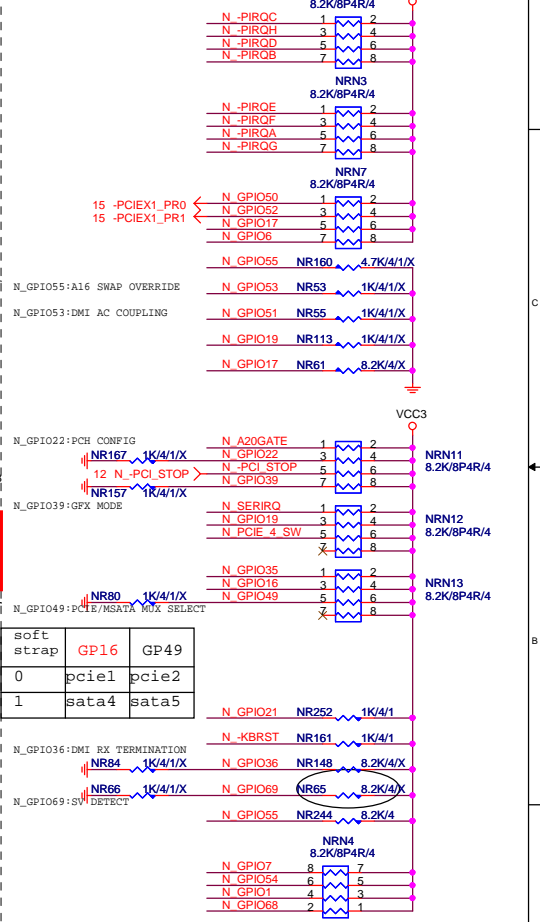
Default int pull up on GP51,  
Default SPI boot devices

BOOT DEVICE	GP51	GP19
LPC	0	0
SPI	float	float

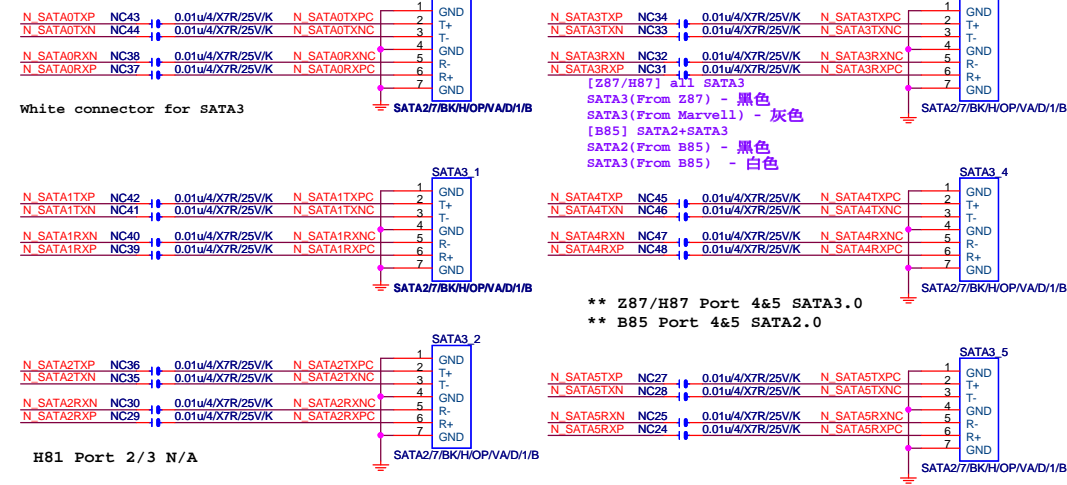
PCH CLK PD



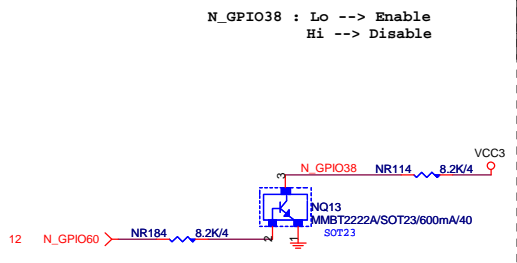
PCH PU/PD



SATA CONNECTOR



GPIO38 Ctrl



**Gigabyte Technology**

Title: PCH HOST , SATA, PCI

Size: Custom

Document Number: GA-Z87-HD3

Date: Friday, March 22, 2013

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Rev: 1.02

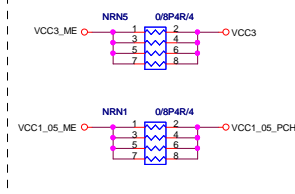
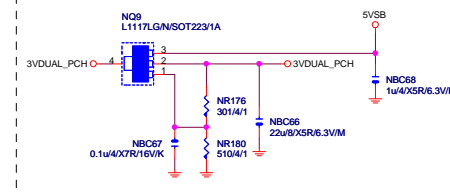
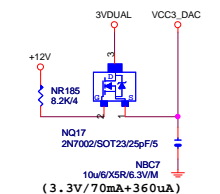




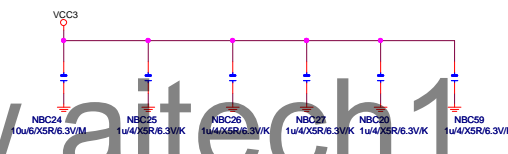
**PCH (I)**



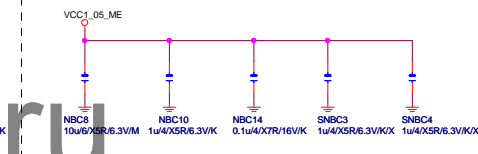
SHT PWR



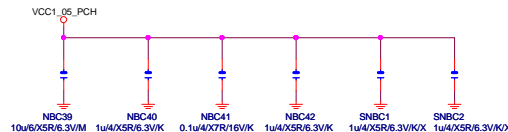
( 3.3V ) ( X6 )



(1.05V) (x5)



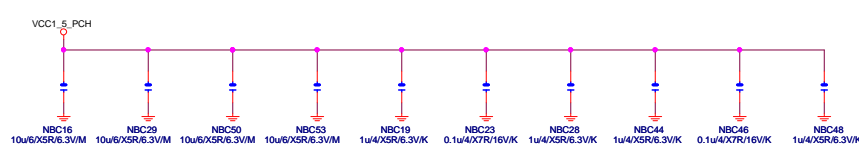
(1.05V) (x6)



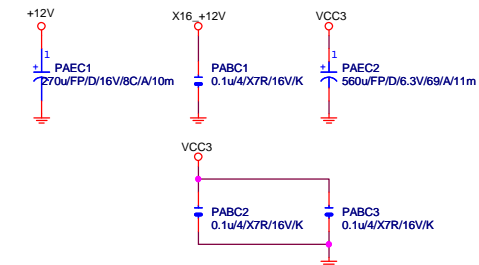
(1.05V)(x2) (3.3V) (x2)



(1.5V) (x10)

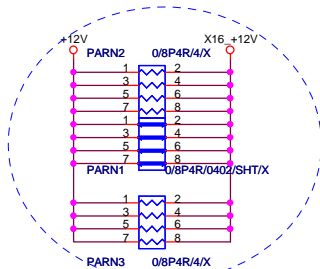


## PCIEX16 CAP



## PCIEX16 PROTECT SHT

```
+12 protect
short-wire test
```



## PCIEX16 AC CAP

PA EXP TXP0	PAC5	0.22u4/XSR/6.3VK	PA EXP TXP0 C
PA EXP TXN0	PAC4	0.22u4/XSR/6.3VK	PA EXP TXN0 C
PA EXP TXP1	PAC6	0.22u4/XSR/6.3VK	PA EXP TXP1 C
PA EXP TXN1	PAC7	0.22u4/XSR/6.3VK	PA EXP TXN1 C
PA EXP TXP2	PAC8	0.22u4/XSR/6.3VK	PA EXP TXP2 C
PA EXP TXN2	PAC9	0.22u4/XSR/6.3VK	PA EXP TXN2 C
PA EXP TXP3	PAC10	0.22u4/XSR/6.3VK	PA EXP TXP3 C
PA EXP TXN3	PAC11	0.22u4/XSR/6.3VK	PA EXP TXN3 C
PA EXP TXP4	PAC12	0.22u4/XSR/6.3VK	PA EXP TXP4 C
PA EXP TXN4	PAC13	0.22u4/XSR/6.3VK	PA EXP TXN4 C
PA EXP TXP5	PAC14	0.22u4/XSR/6.3VK	PA EXP TXP5 C
PA EXP TXN5	PAC15	0.22u4/XSR/6.3VK	PA EXP TXN5 C
PA EXP TXP6	PAC16	0.22u4/XSR/6.3VK	PA EXP TXP6 C
PA EXP TXN6	PAC17	0.22u4/XSR/6.3VK	PA EXP TXN6 C
PA EXP TXP7	PAC18	0.22u4/XSR/6.3VK	PA EXP TXP7 C
PA EXP TXN7	PAC18	0.22u4/XSR/6.3VK	PA EXP TXN7 C
PA EXP TXP8	PAC20	0.22u4/XSR/6.3VK	PA EXP TXP8 C
PA EXP TXN8	PAC21	0.22u4/XSR/6.3VK	PA EXP TXN8 C
PA EXP TXP9	PAC22	0.22u4/XSR/6.3VK	PA EXP TXP9 C
PA EXP TXN9	PAC23	0.22u4/XSR/6.3VK	PA EXP TXN9 C
PA EXP TXP10	PAC24	0.22u4/XSR/6.3VK	PA EXP TXP10 C
PA EXP TXN10	PAC25	0.22u4/XSR/6.3VK	PA EXP TXN10 C
PA EXP TXP11	PAC26	0.22u4/XSR/6.3VK	PA EXP TXP11 C
PA EXP TXN11	PAC27	0.22u4/XSR/6.3VK	PA EXP TXN11 C
PA EXP TXP12	PAC28	0.22u4/XSR/6.3VK	PA EXP TXP12 C
PA EXP TXN12	PAC29	0.22u4/XSR/6.3VK	PA EXP TXN12 C
PA EXP TXP13	PAC30	0.22u4/XSR/6.3VK	PA EXP TXP13 C
PA EXP TXN13	PAC31	0.22u4/XSR/6.3VK	PA EXP TXN13 C
PA EXP TXP14	PAC32	0.22u4/XSR/6.3VK	PA EXP TXP14 C
PA EXP TXN14	PAC33	0.22u4/XSR/6.3VK	PA EXP TXN14 C
PA EXP TXP15	PAC34	0.22u4/XSR/6.3VK	PA EXP TXP15 C
PA EXP TXN15	PAC35	0.22u4/XSR/6.3VK	PA EXP TXN15 C

PCI-E REV:1.1--&gt; 2.5GHZ

PCE-E X1(單向) BANDWIDTH=2.5GHz\*(8b/10b)=2Gb/s=250MB/s

PCE-E X1(雙向) BANDWITH=2.5GHz\*(8b/10b)X2=4Gb/s=500MB/s

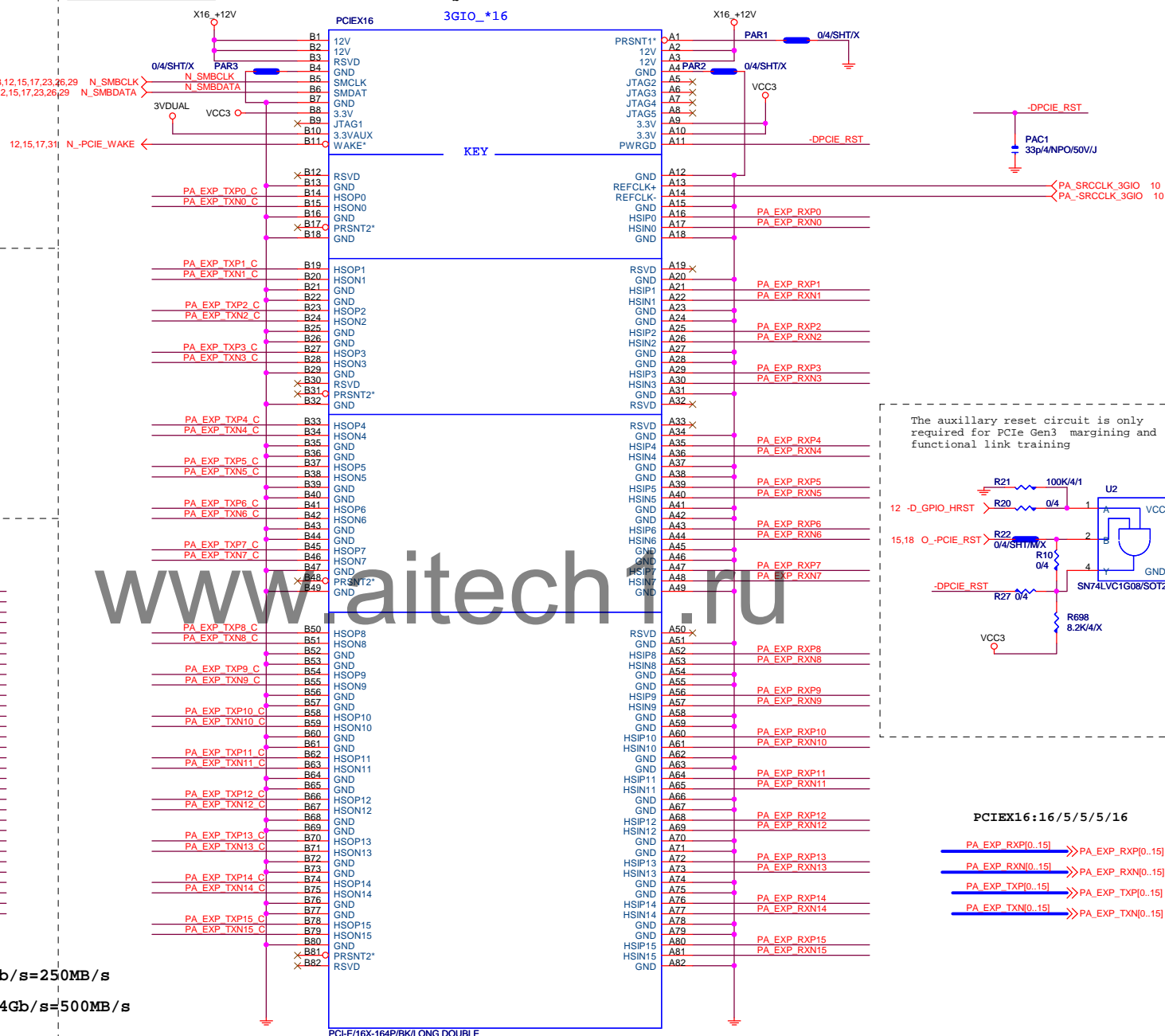
PCE-E X16(單向) BANDWITH=2.5GHz\*(8b/10b)X16=32Gb/s=4GB/s

PCE-E X16(雙向) BANDWITH=2.5GHz\*(8b/10b)X16X2=64Gb/s=8GB/s

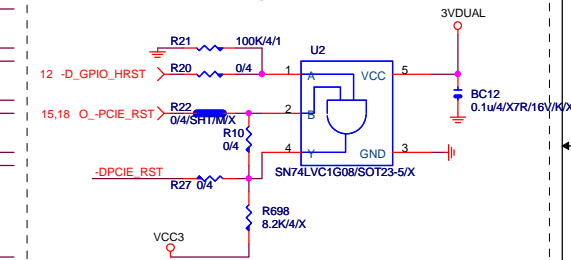
PCI-E REV:2.0--&gt; 5GHZ

PCIEX16 SLOT

## PCIESLOT-164DN-Q



The auxillary reset circuit is only required for PCIe Gen3 margining and functional link training



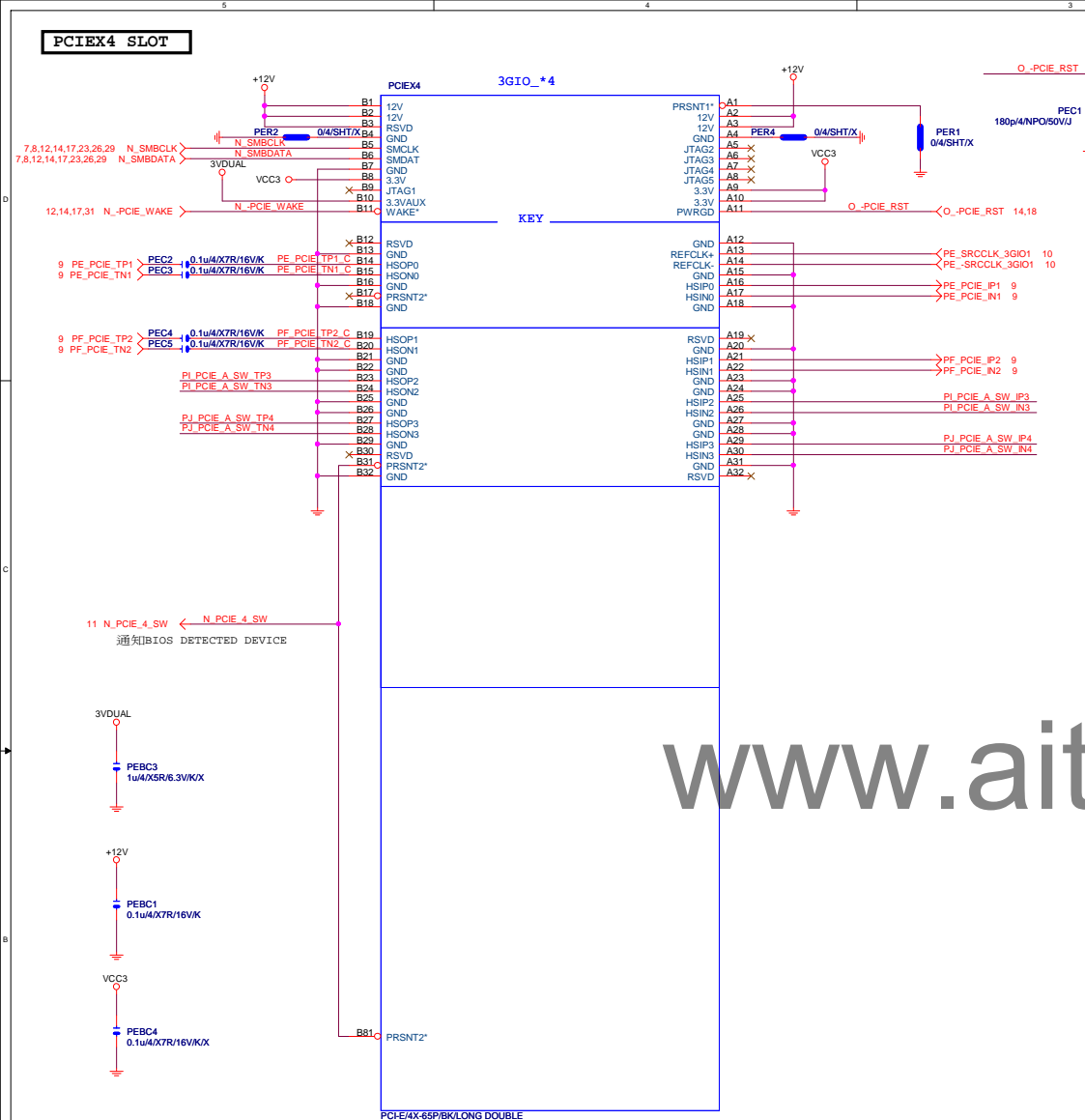
PCIEX16:16/5/5/5/16

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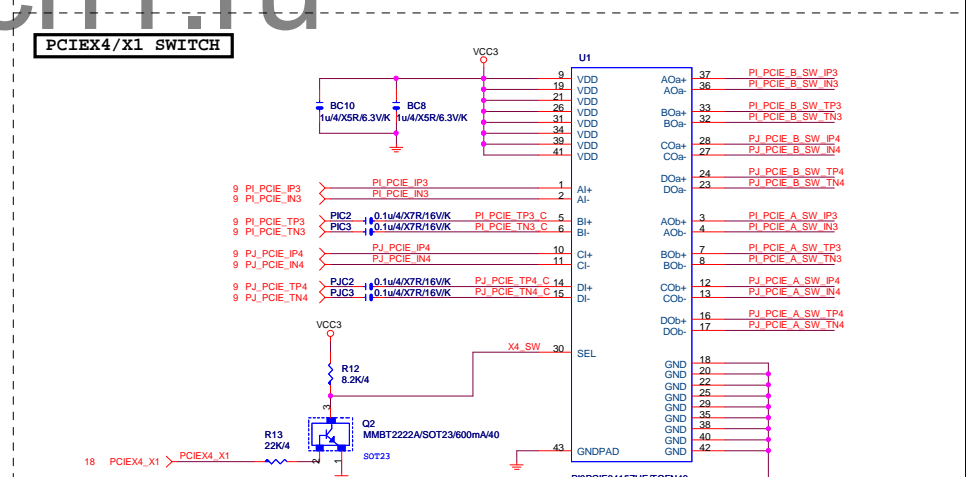
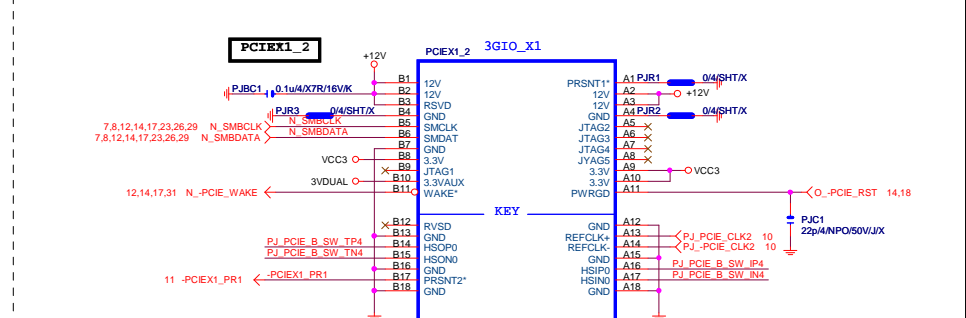
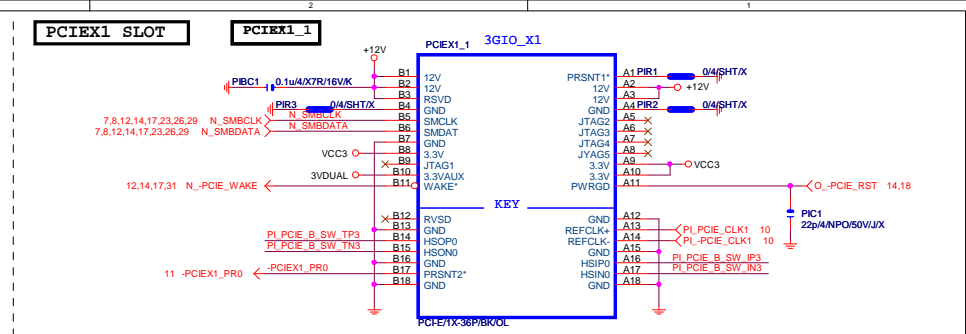
PA_EXP_RXP[0..15] >> PA_EXP_RXP[0..15] 4
PA_EXP_RXN[0..15] >> PA_EXP_RXN[0..15] 4
PA_EXP_TXP[0..15] >> PA_EXP_TXP[0..15] 4
PA_EXP_TXN[0..15] >> PA_EXP_TXN[0..15] 4

```

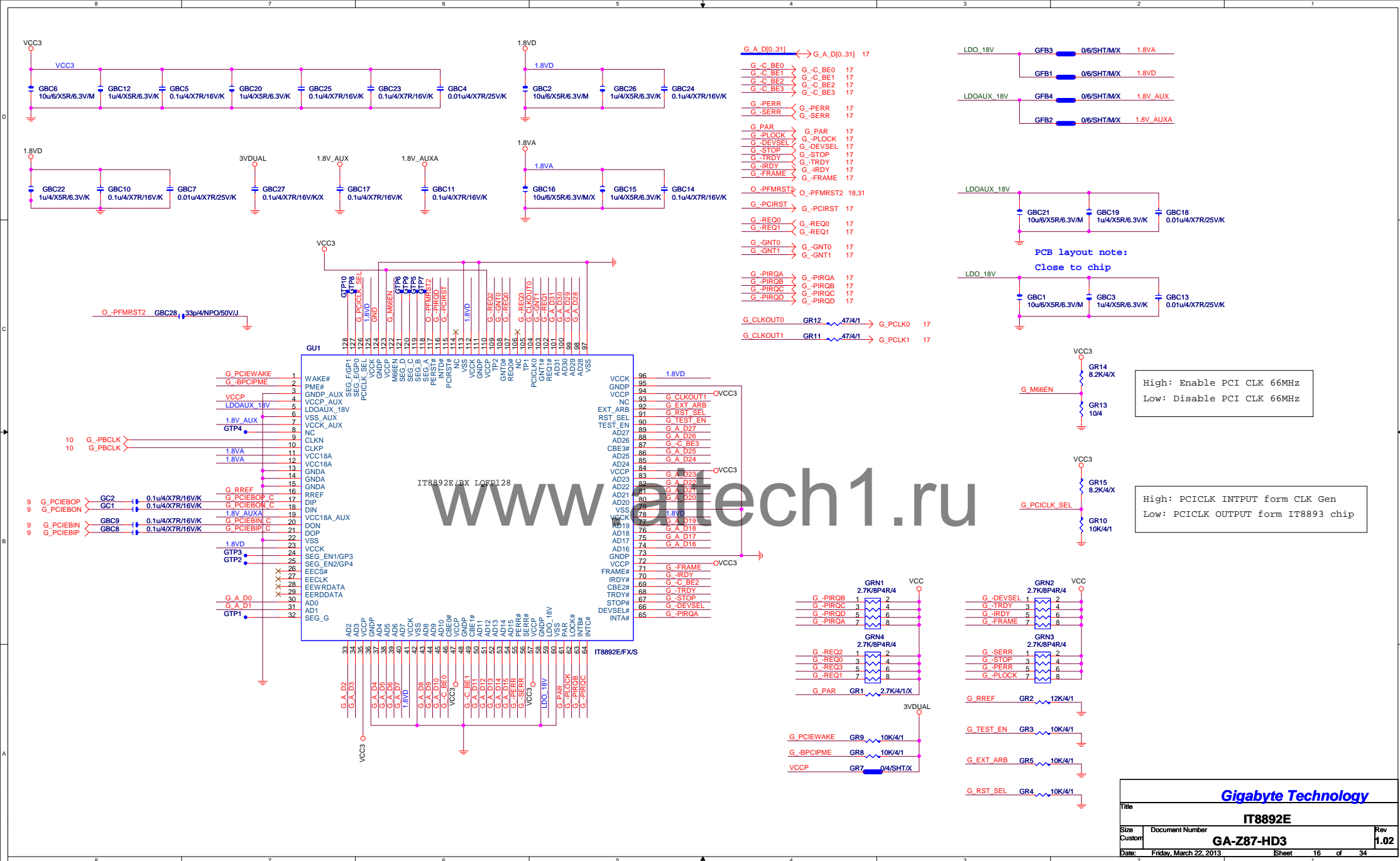
<b>Gigabyte Technology</b>			
Title <b>PCI EXPRESS * 16</b>			
Size Custom	Document Number <b>GA-Z87-HD3</b>		Rev <b>1.02</b>
Date:	Friday, March 22, 2013	Sheet 14 of 34	



	N_PCIE_4_SW (PCH GPIO48)	PCIEX4_X1 (SIO_GPIO26)
PCIEX4 No devices	H	H
PCIEX4 -> X1	H	H
PCIEX4 Have devices	L	L
PCIEX4 -> X4	L	L
PCIEX1_1/2 --> N/A		

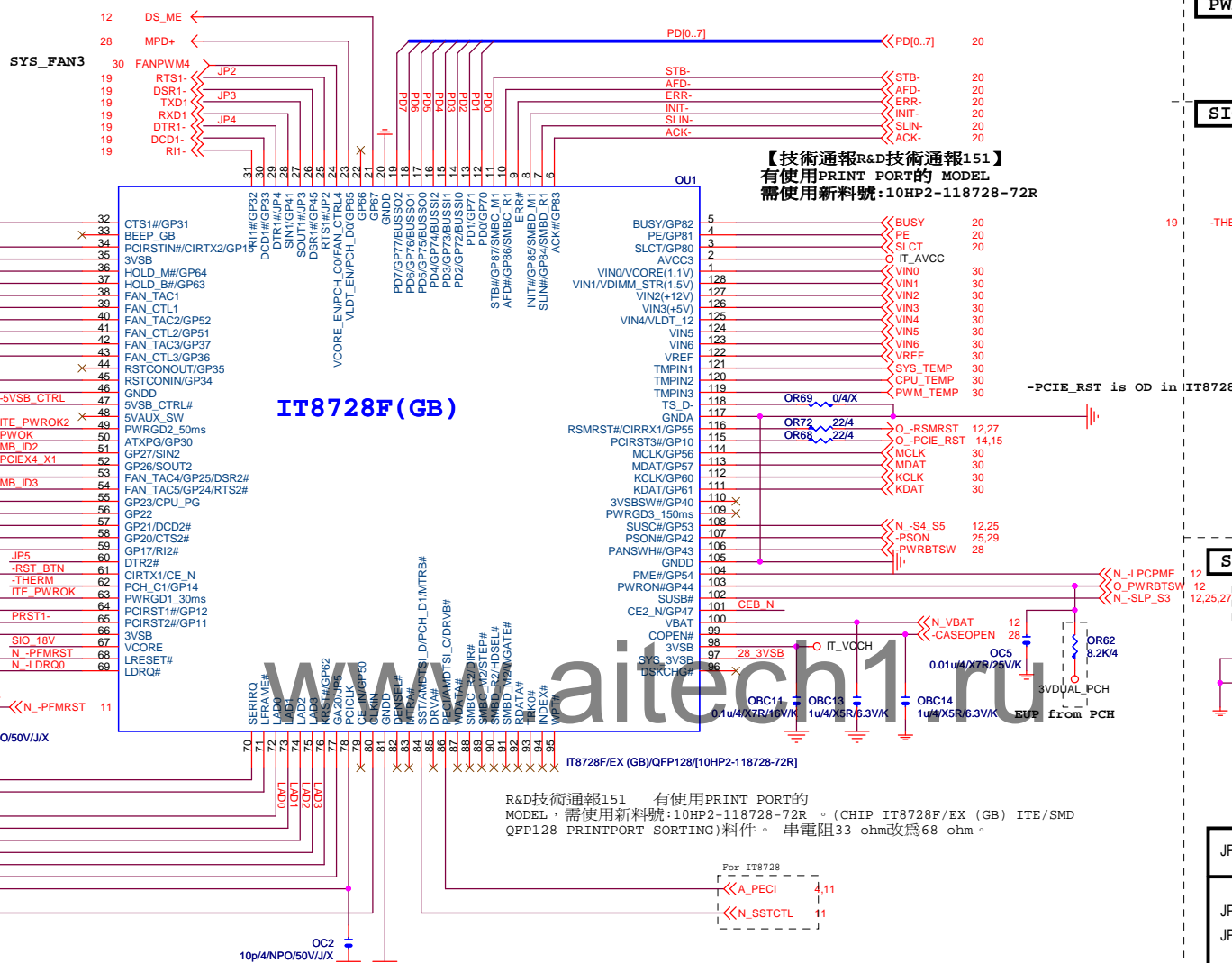


Function	SEL
xI--> x0A	L;PCIEX4 SLOT-->X1
xI--> x0B	H;PCIEX4 SLOT-->X4

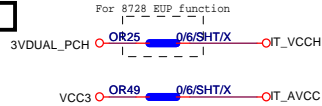




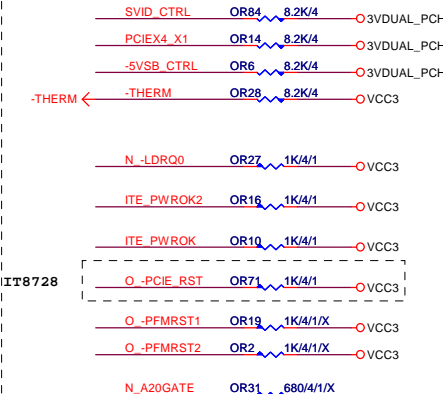
## SIO IT8728F



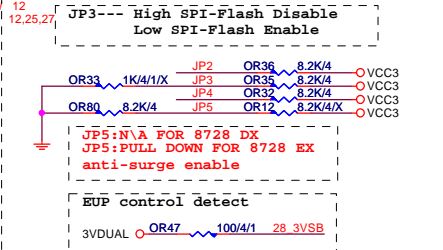
	PWR	SHT
1	1	1
2	1	1
3	1	1
4	1	1
5	1	1
6	1	1
7	1	1
8	1	1
9	1	1
10	1	1
11	1	1
12	1	1
13	1	1
14	1	1
15	1	1
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92	1	1
93	1	1
94	1	1
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98	1	1
99	1	1
100	1	1



SIO	PU
-----	----



SIO STRAP

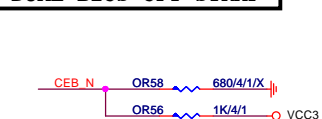


JP4	1	k8 power sequency function is Disable
	0	k8 power sequency function is Enable
JP3	1 1	The default value of EC Index 63h/6Bh/73h is 80h
	0 1	The default value of EC Index 63h/6Bh/73h is F0h
JP5	1 0	The default value of EC Index 63h/6Bh/73h is 00h
	0 0	The default value of EC Index 63h/6Bh/73h is 40h

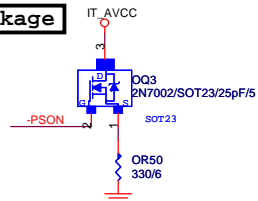
## IT8728F NOTE

	IT8728
PIN121	VCORE_EN/PCH_C0
PIN120	VLDT_EN/PCH_D0
PIN19	ATXPG
PIN31	PCH_C1
PIN53	SST/AMDTSL_D/MTB# /PCH_D1
PIN55	PECI/AMDTSL_C/DRV#
PIN66	SYS_3VSB
PIN70	GP47
PIN95	VIN2 (VCC5)
PIN96	VIN1 (VCC12)
PIN97	VIN1/VDIMM_STR(1.5V)
PIN98	VINO/VCORE(1.1V)/NC

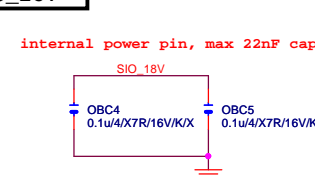
## DUAL BIOS OPT STRAP



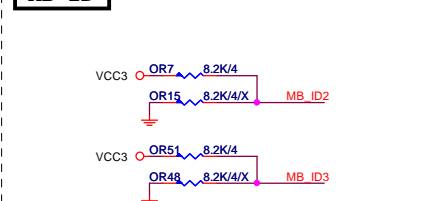
## Power leakage



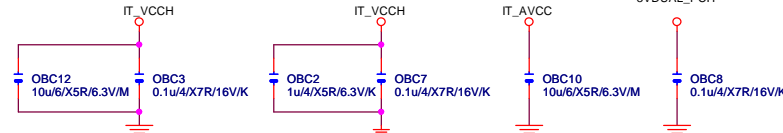
## SIO 18V



## MB ID



## SIO CAP

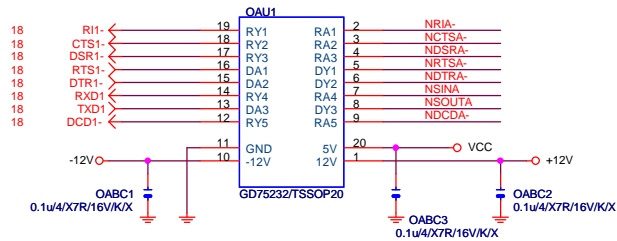


## Gigabyte Technology

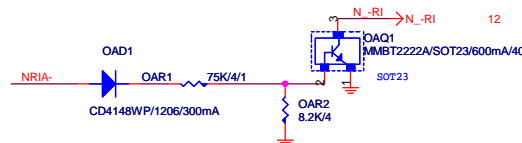
Title			
ITE 8728 LPC IO			
Size B	Document Number	GA-Z87-HD3	Rev 1.02
Date:	Friday, March 22, 2013	Sheet	18 of 34



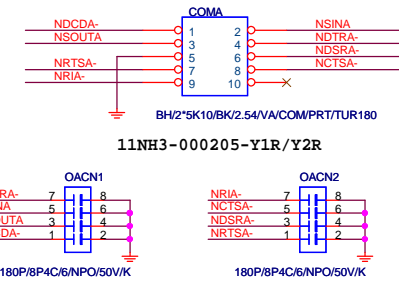
## COMA



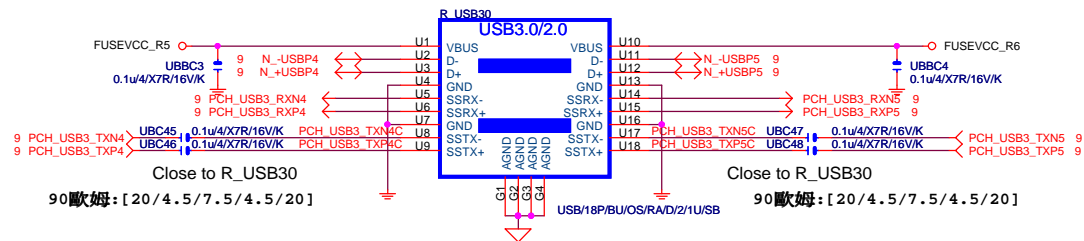
## COM RI



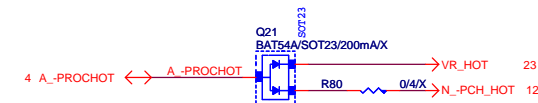
## COM BUFFER



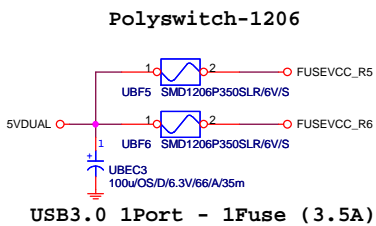
## USB30\_20 CONNECT



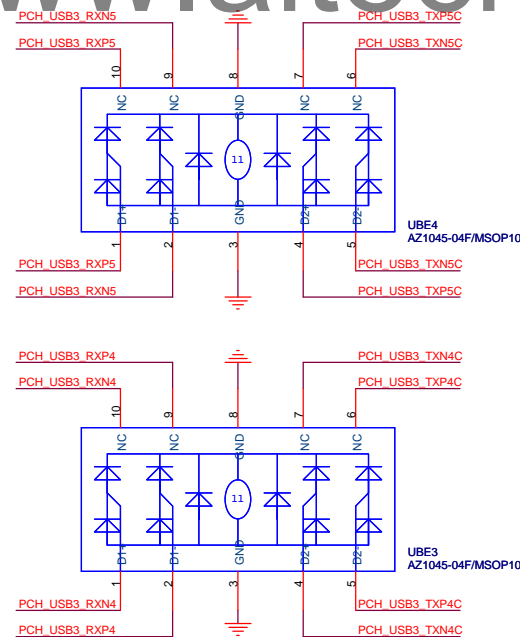
## -PROHOT



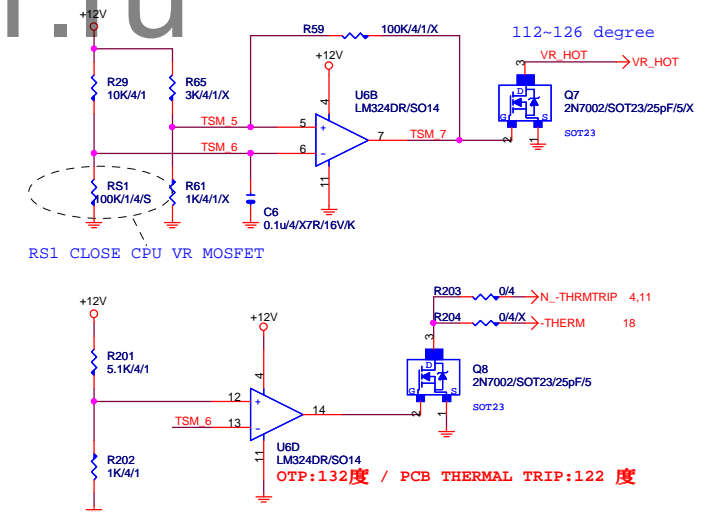
## USB30 PWR



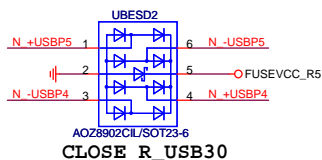
## USB30 ESD PROTECT



## -PROHOT



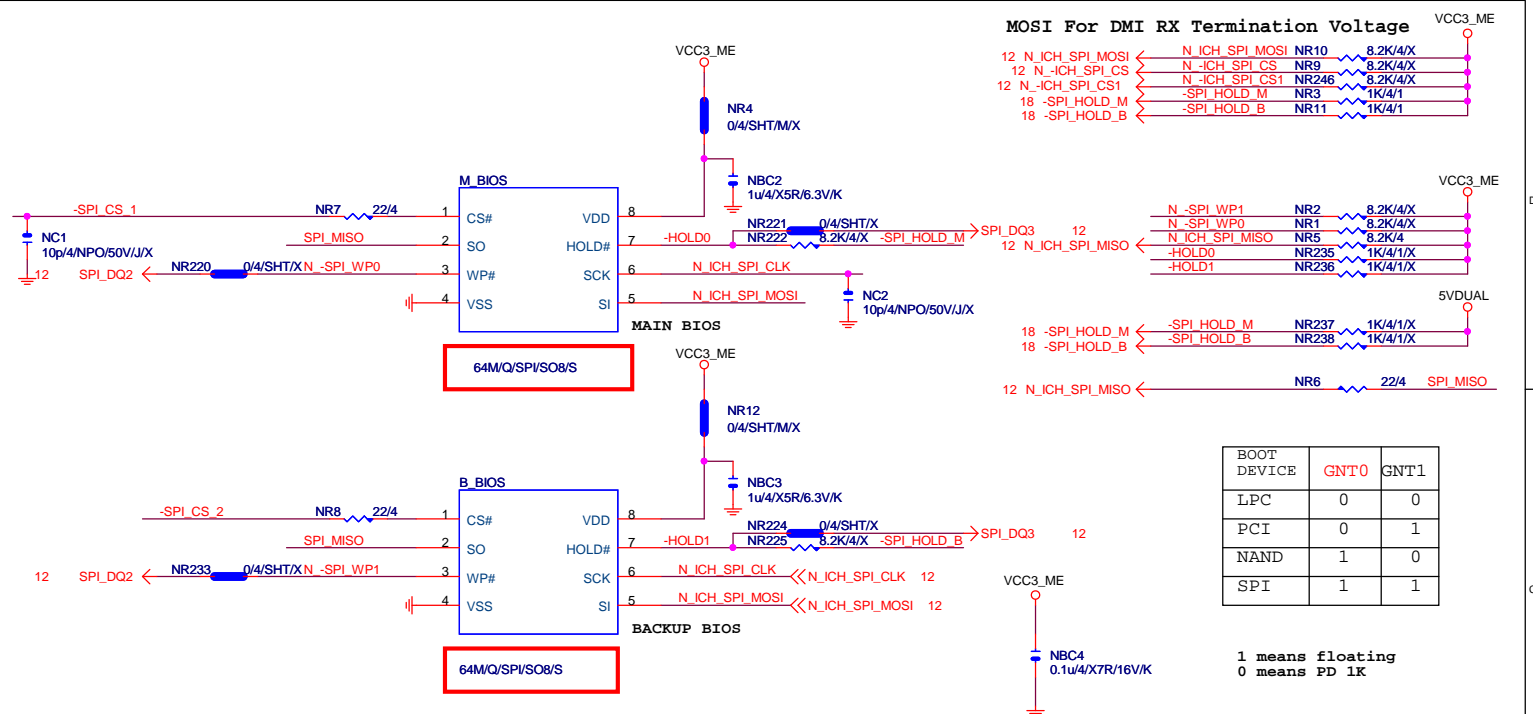
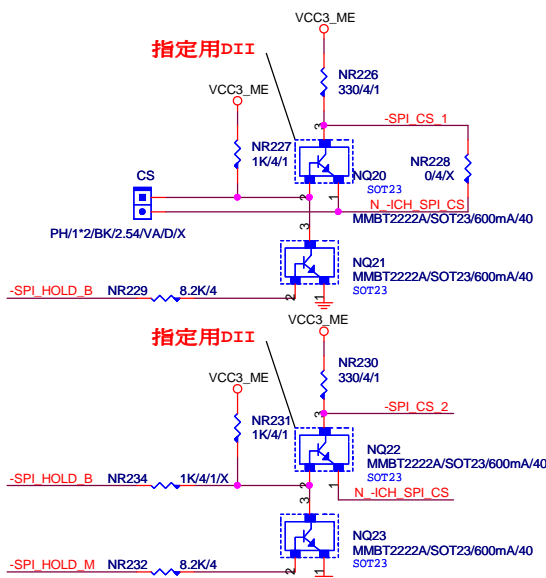
## USB20 ESD PROTECT



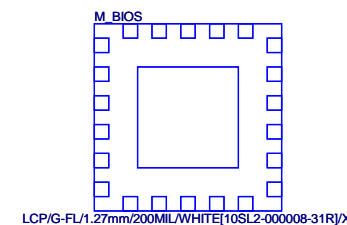
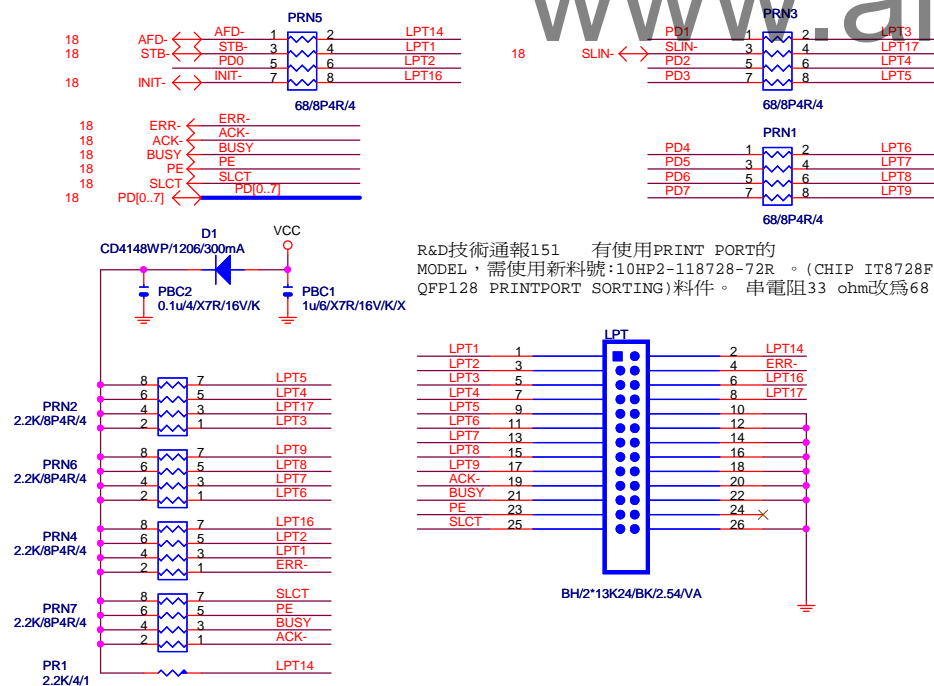
Gigabyte Technology

Title			
COM/ PROHOT/ R_USB			
Size	Document Number	Rev	
Custom		GA-Z87-HD3	
Date:	Friday, March 22, 2013	Sheet	19 of 34

## DUAL BIOS

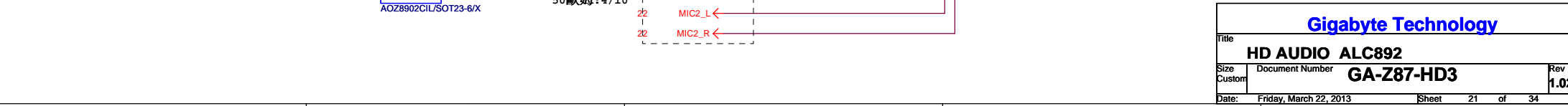


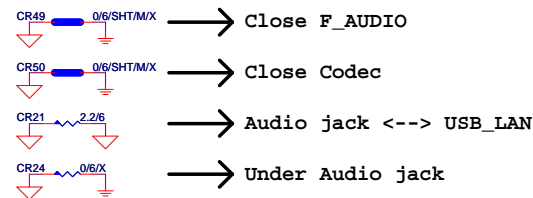
## LPT PORT



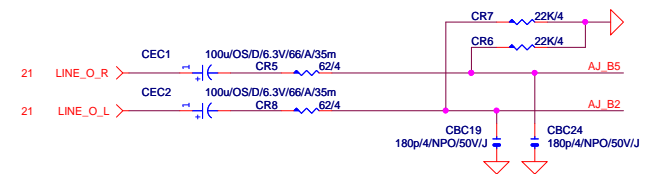


Pin 1 to 6 connection diagram for the AOZ8902C/L/SOT23-6/X. The diagram shows a 6-pin package with pins 1, 2, 3, 4, 5, and 6. Pin 1 is connected to LINE2\_L. Pin 2 is connected to a triangle symbol. Pin 3 is connected to MIC2\_R. Pin 4 is connected to MIC2\_L. Pin 5 is connected to 5VDDA. Pin 6 is connected to LINE2\_R. The package is labeled CSD1 and AOZ8902C/L/SOT23-6/X.





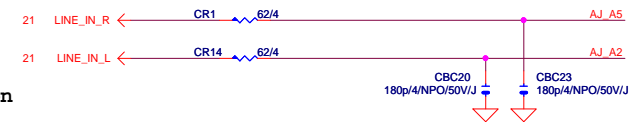
## LINE-OUT



## LINE-IN

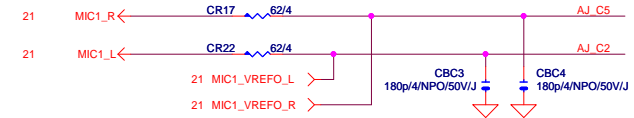
Verify MIC function  
in LINE-in

Only reserved for ALC888

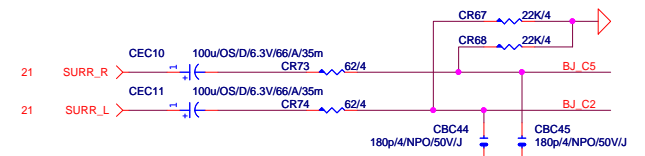


For 889A/888

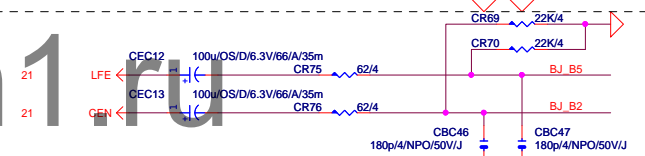
## MIC-IN



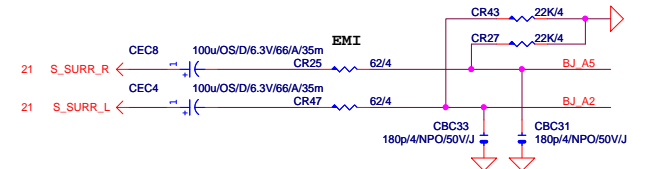
## SURROUND



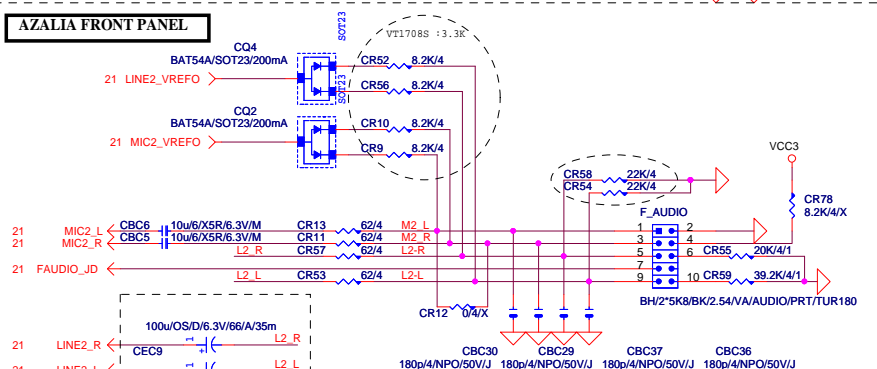
## CEN/LFE



## SURR BACK



## AZALIA FRONT PANEL



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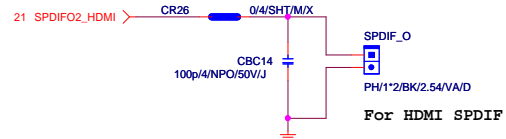
AUDIO JACK

GA-Z87-HD3

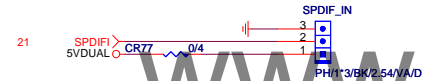
Rev 1.02

Date: Friday, March 22, 2013 Sheet 22 of 34

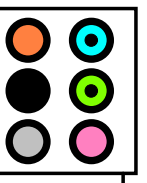
## SPDIF\_OUT



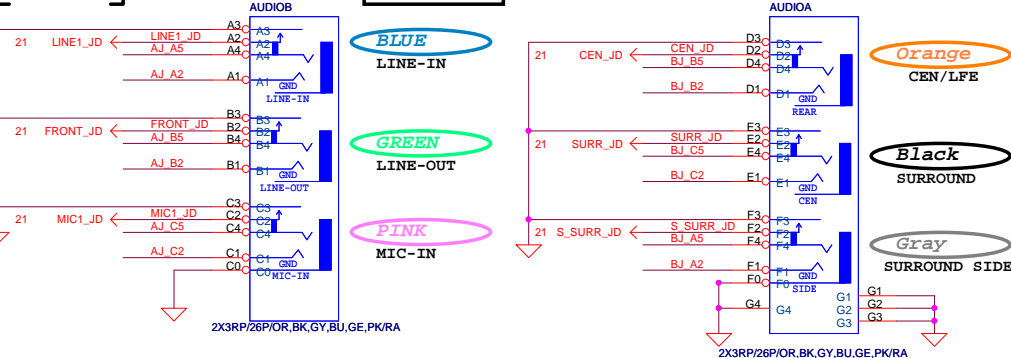
## SPDIF\_IN



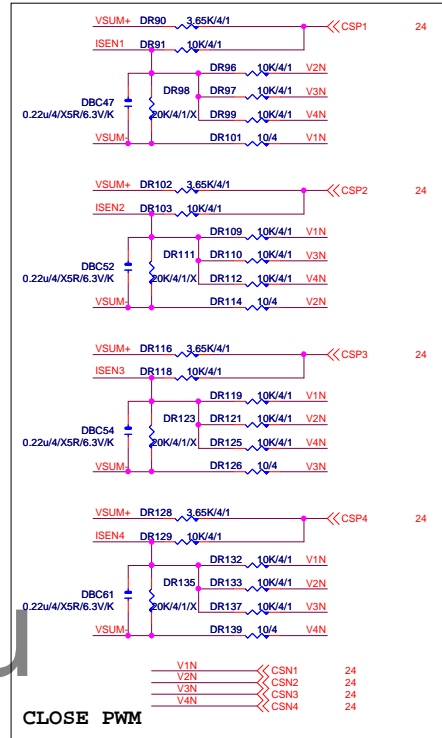
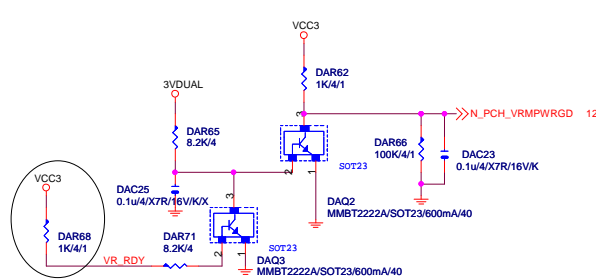
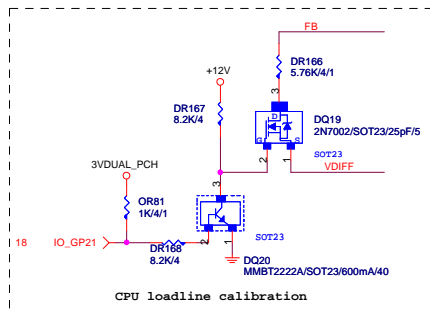
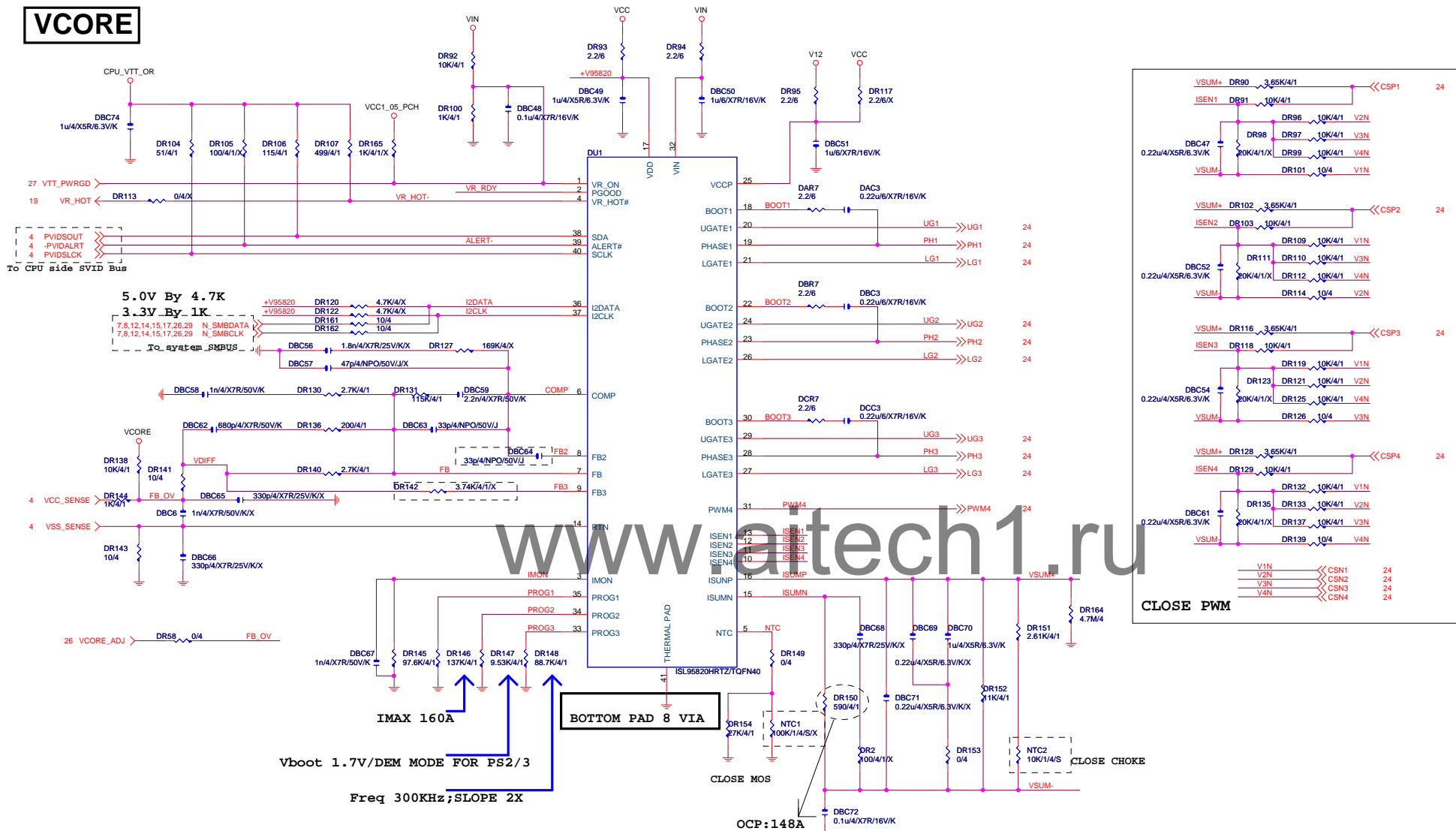
## AZALIA JACK



## AZALIA JACK

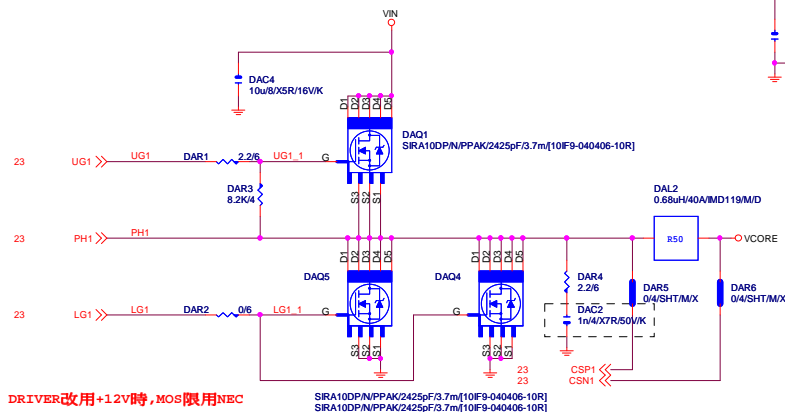


# VCORE

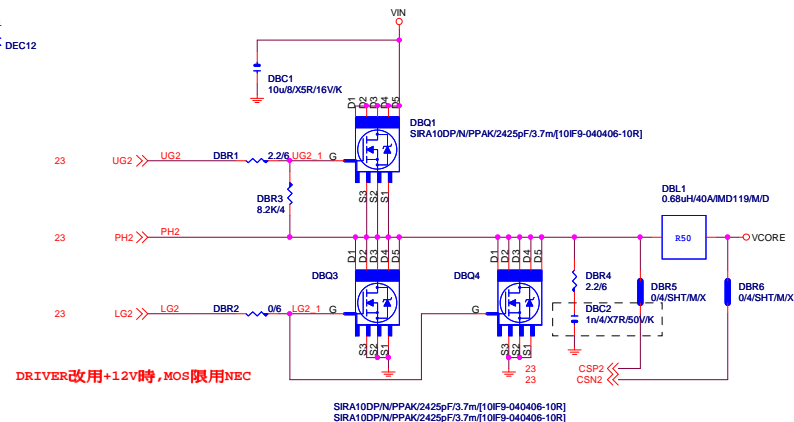


# VCORE

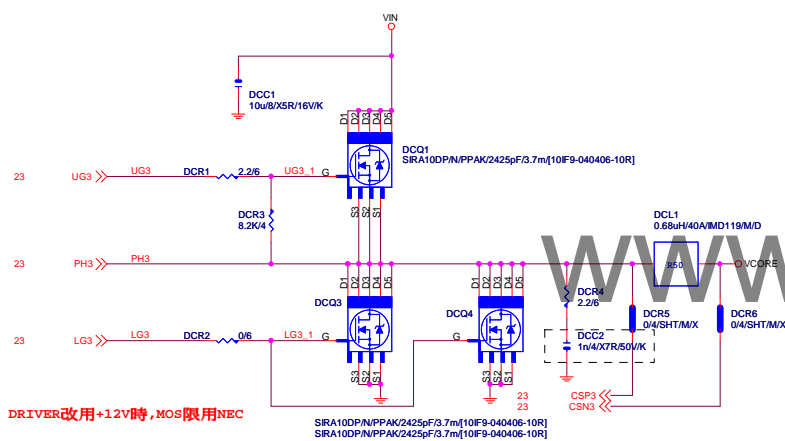
[1]



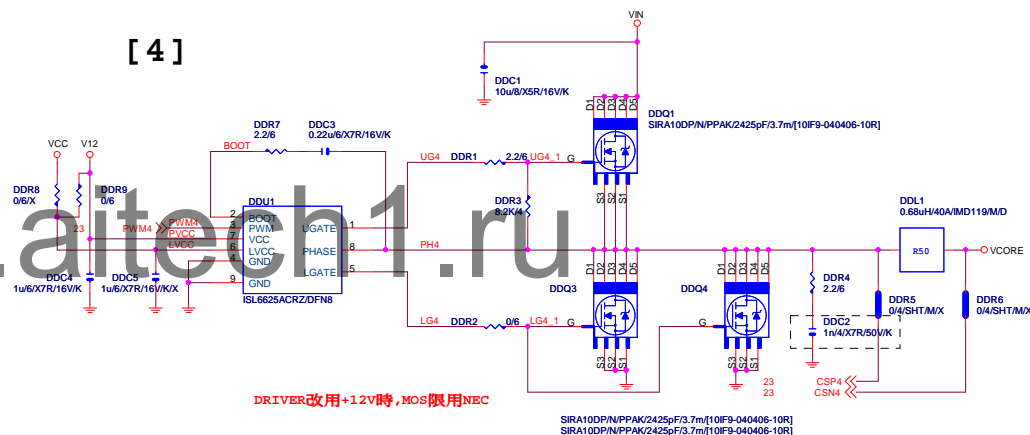
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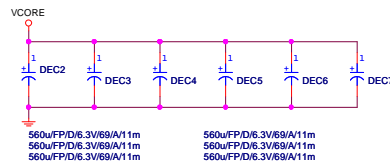
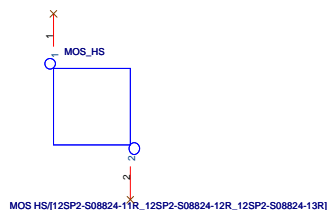
[3]



[4]



## MOSFET HEATSINK

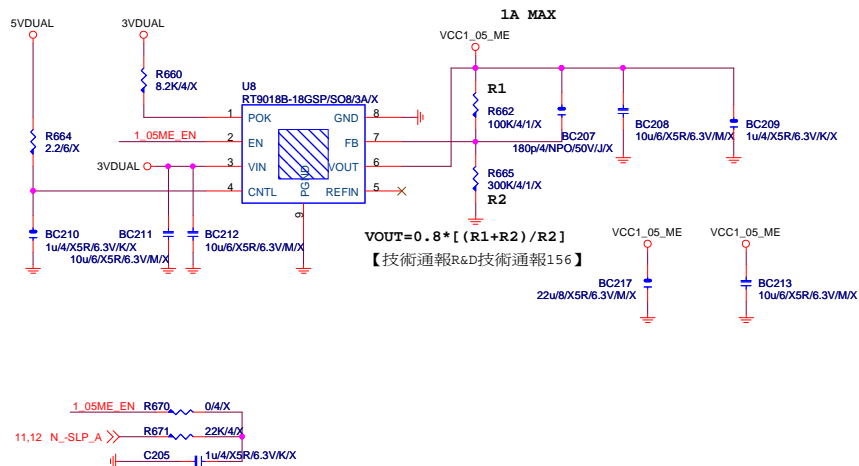


Gigabyte Technology

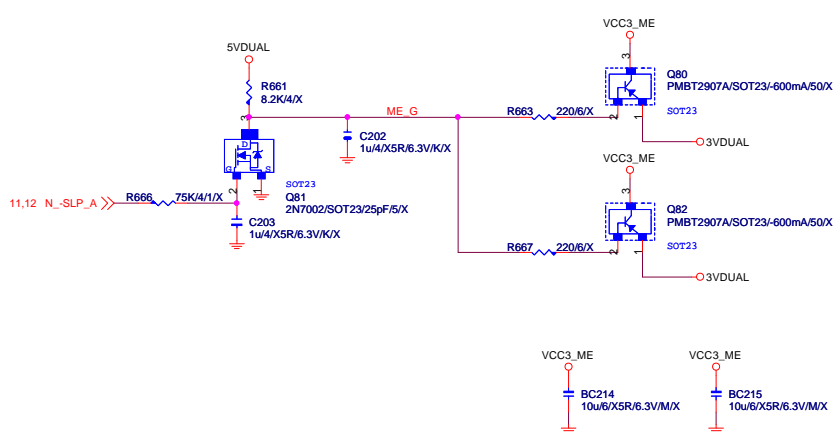
Title			ISL95820_2
Size			Document Number
Custom			GA-Z87-HD3
Date	Friday, March 22, 2013	Sheet	24 of 34

Rev 1.02

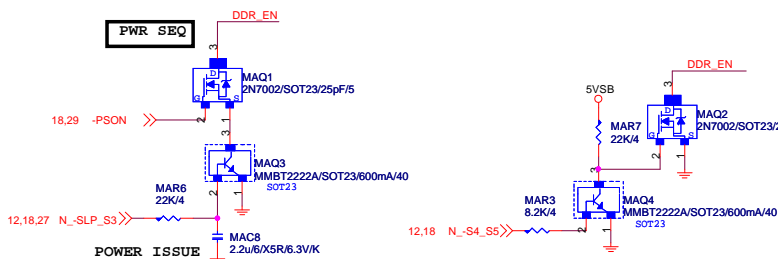
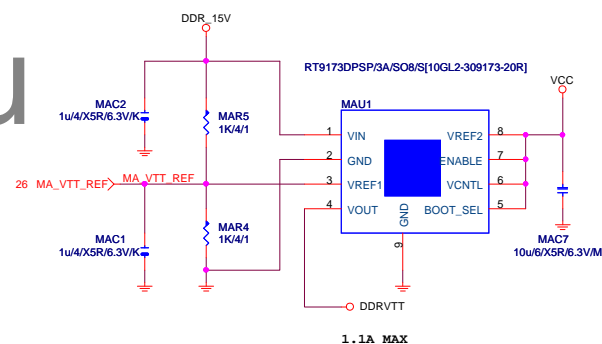
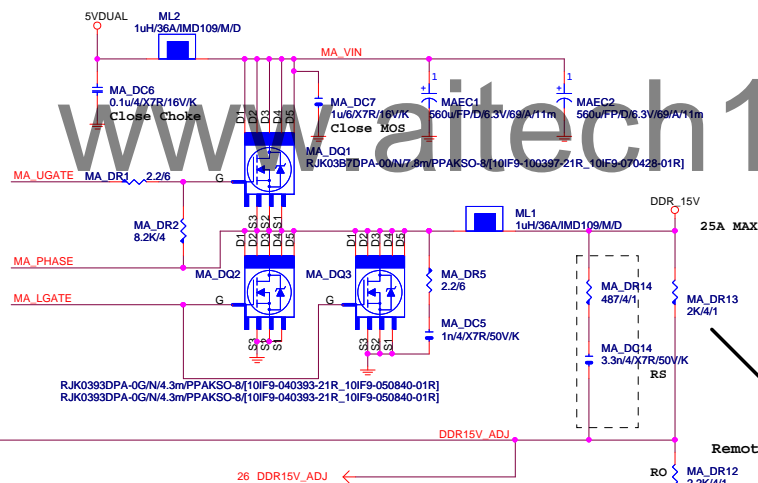
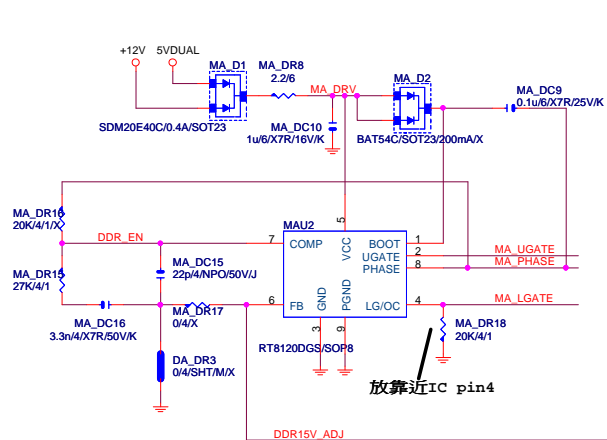
VCC1\_05\_ME



VCC3\_ME

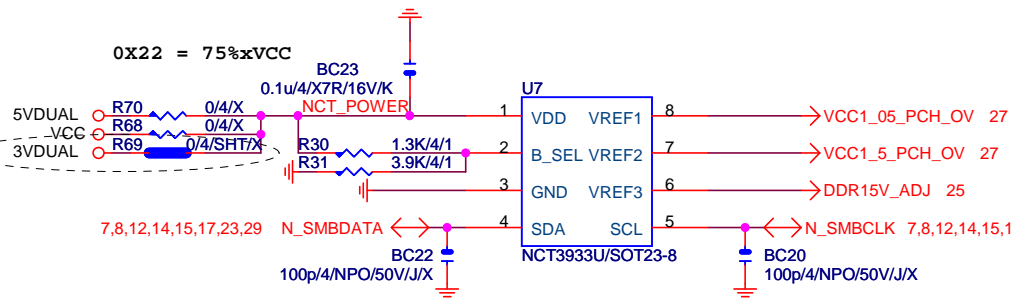


**DDR\_15V**

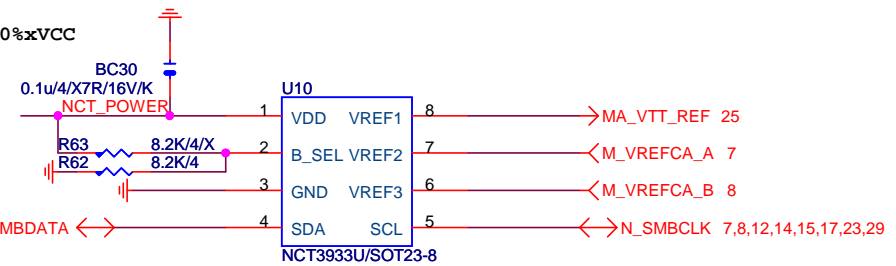


VIN=5V, VOUT=1.5V, IOUT=25A, PHASE=1 1.527V  
IRMS=11.45A  
560u/FP/D/6.3V/68/8m RIPPLE CURRENT=4.7A  
Coefficient=1.7(85°C), 1(105°C)  
VIN Ripple current=4.7X1.7=7.99A(85°C)  
-->故固態電容須2X7.99=15.98>11.45A  
  
OCP:35.82A for Rds=6.7m for vishay@4.5V  
OCP:72.727A for Rds=3.3m for renesas@10V  
OCP:48A=Roset\*Iocset / Rds(on)  
=12K\*10uA / [5/5]

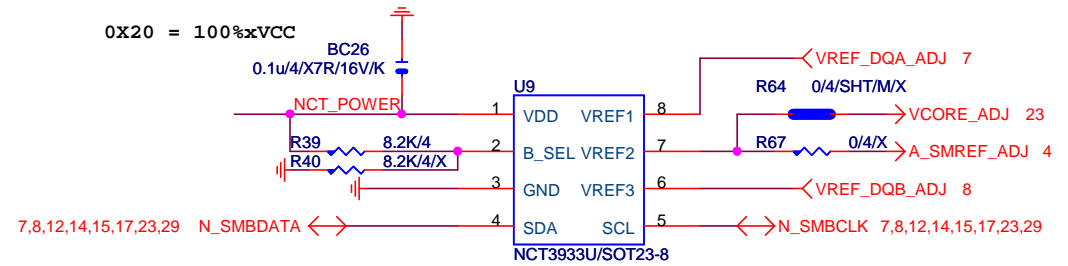
# OVER VOLTAGE



0X2A = 0%xVCC



0X20 = 100%xVCC



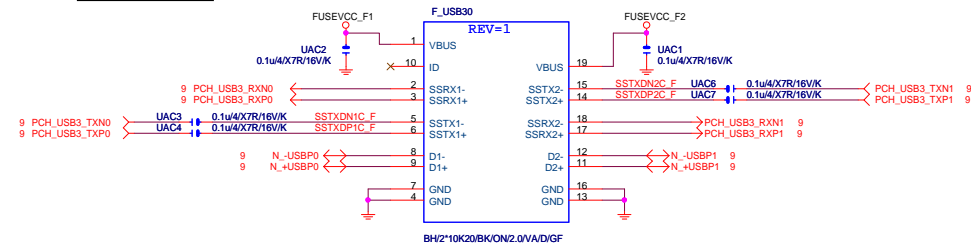
NCT3933	0X2A	0X20	0X22
VREF1	DDRVTT	VREF_DDRA_DQ	PCH Core
VREF2	VREF_DDRA_CA	N/A	VCC1_5_PCH
VREF3	VREF_DDRA_CA	VREF_DDRB_DQ	SMREF

**Gigabyte Technology**

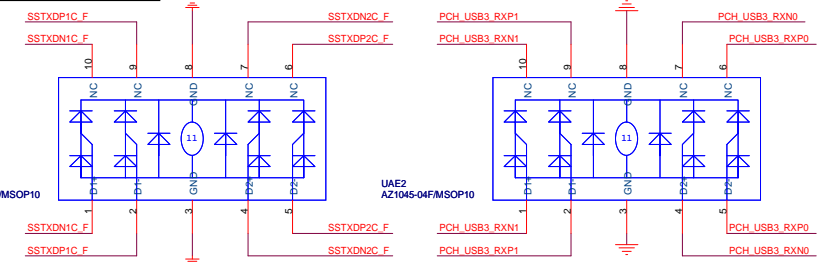
Title			CPU CORE VR-2
Size	Document Number	GA-Z87-HD3	
Custom		Date: Friday, March 22, 2013	Rev 1.02
		Sheet 26 of 34	



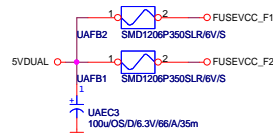
## Front USB3.0



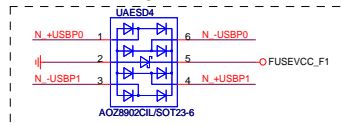
F\_USB30 ESD PROTECT



## F\_USB30 PWR

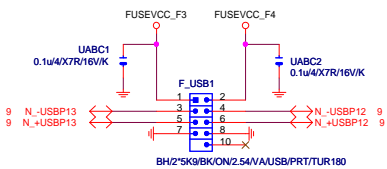


BLUE

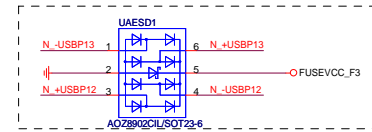


Close to connector

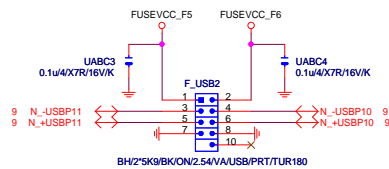
FRONT USB1



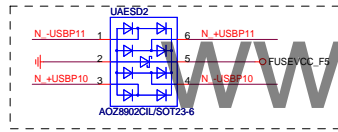
Close to connector



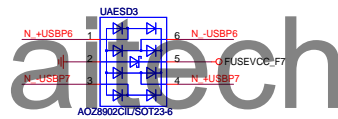
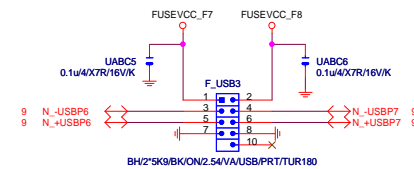
FRONT USB2



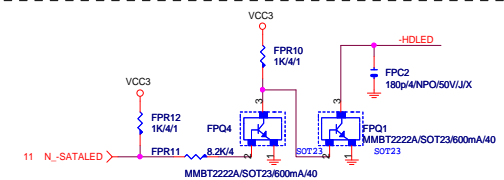
Close to connector



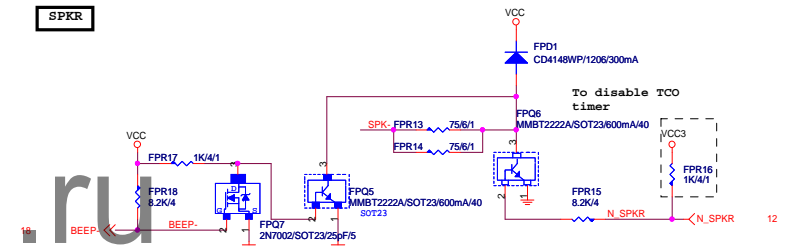
FRONT USB3



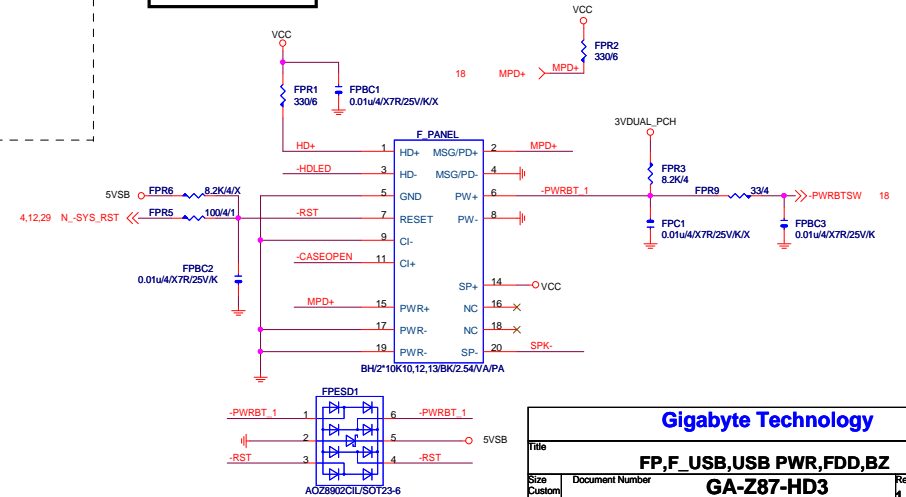
## SATA LED



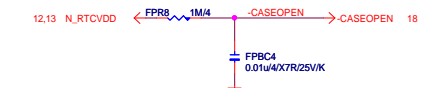
## SPKR



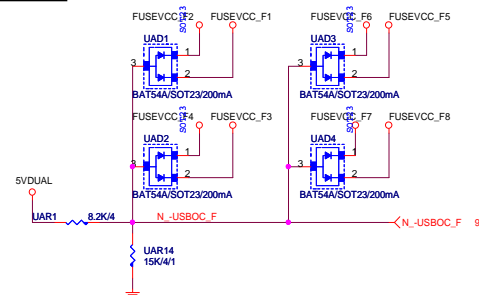
## INTEL FRONT PANEL



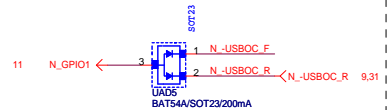
## CASE OPEN



## -USB0C\_F

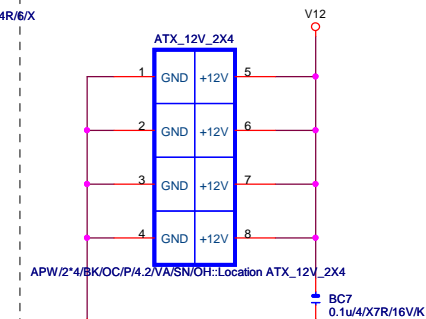


F\_USB POWER PROTECT

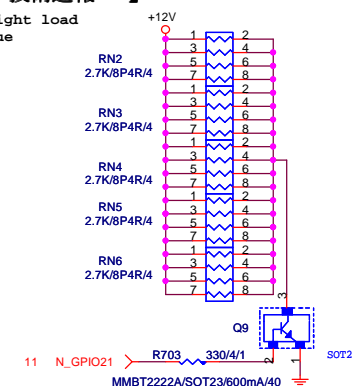
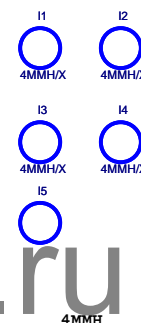




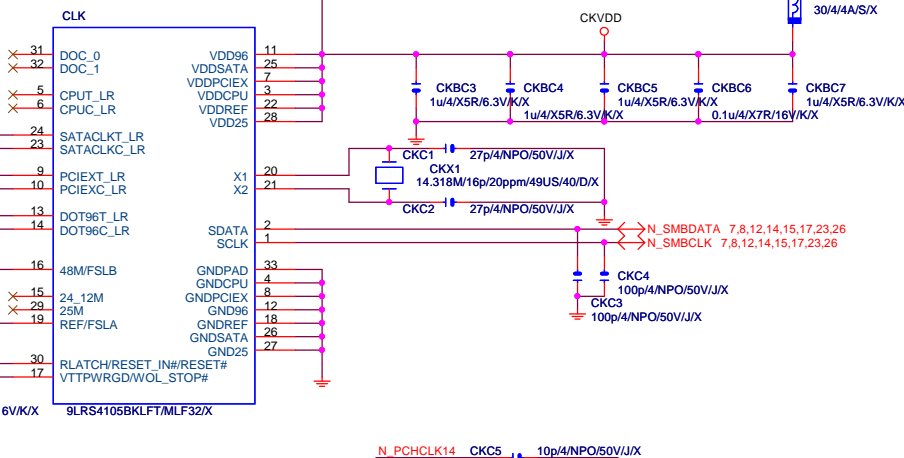
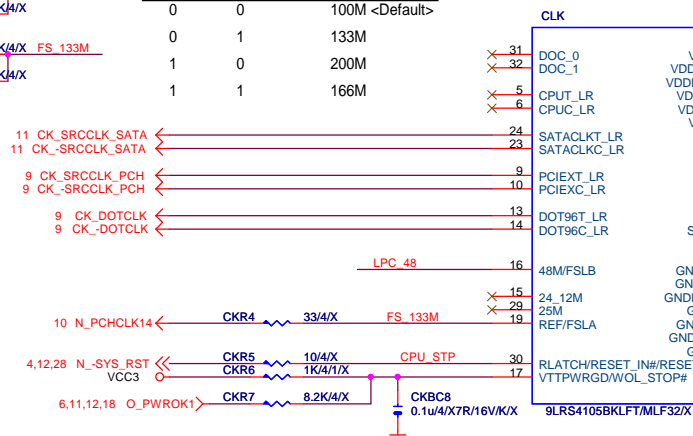
ATXX4 POWER CONNECTOR



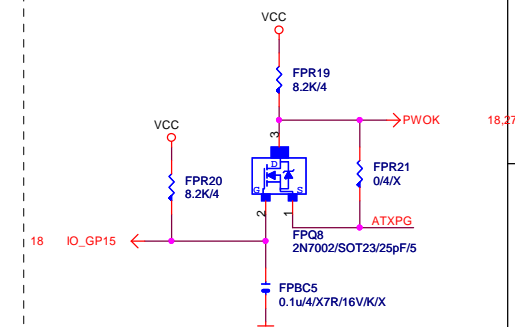
【技術通報R&amp;D技術通報153】



### CPU Frequency Selection



## 【技術通報R&amp;D技術通報154】



## Gigabyte Technology

Title			
<b>ATX POWER CONNECTOR</b>			
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Rev 0.2 modify

VREF

OR73 10K/4/1

R674 8.2K/4

R675 8.2K/4

R679 8.2K/4

OC6 1u4/5R/6.3V/K

OC7 1u4/5R/6.3V/K

RS\_SYS 10K/1/4/S

RS\_PWM 1u4/5R/6.3V/K

C232 1u4/5R/6.3V/K

VCORE\_MOS

Close SIO

Close CPU

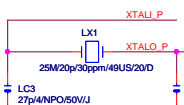
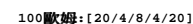
The division voltage of VIN2 & VIN3 must be around 2.9V

[illegible][illegible][illegible]

**Linear SYS FAN**

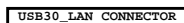


## LAN:INTEL I217



80歐姆:[15/5/5/5/15]

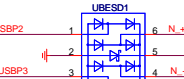
SRCCLK 50MHz: [18/4/10/4/18]



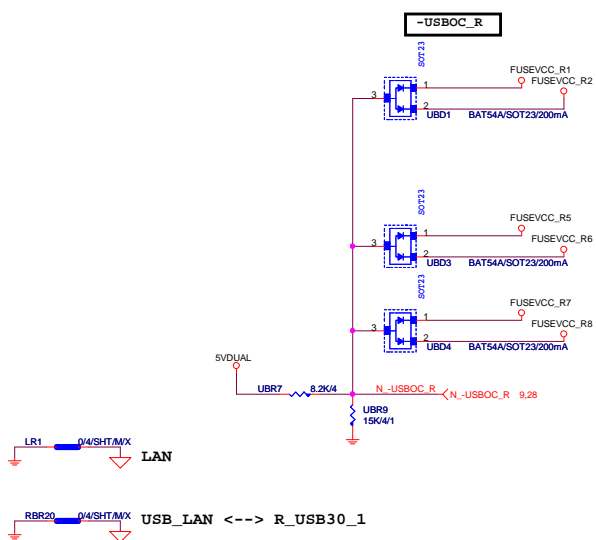
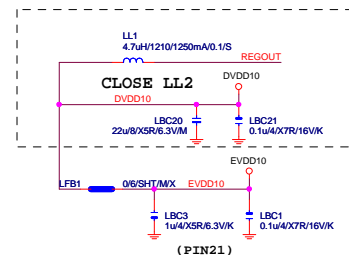
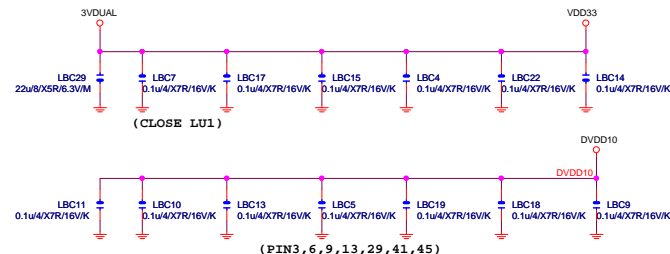
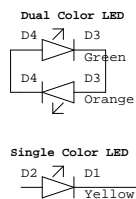
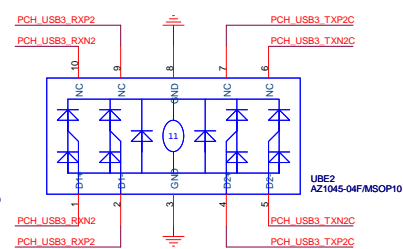
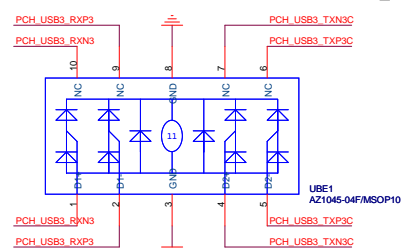
100歐姆:[20/4/8/4/20]

USB30\_LAN  
USB3+LAN/1G/GQ Y/QS/RA/D/G30/11NR6-702009-K1R1

90 歐姐:[15/4.5/7.5/4.5/15]

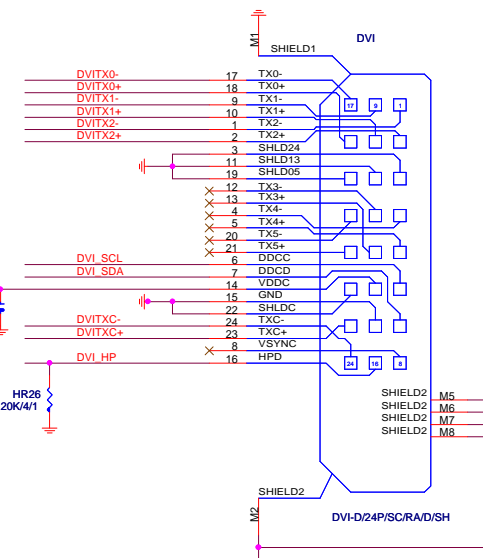
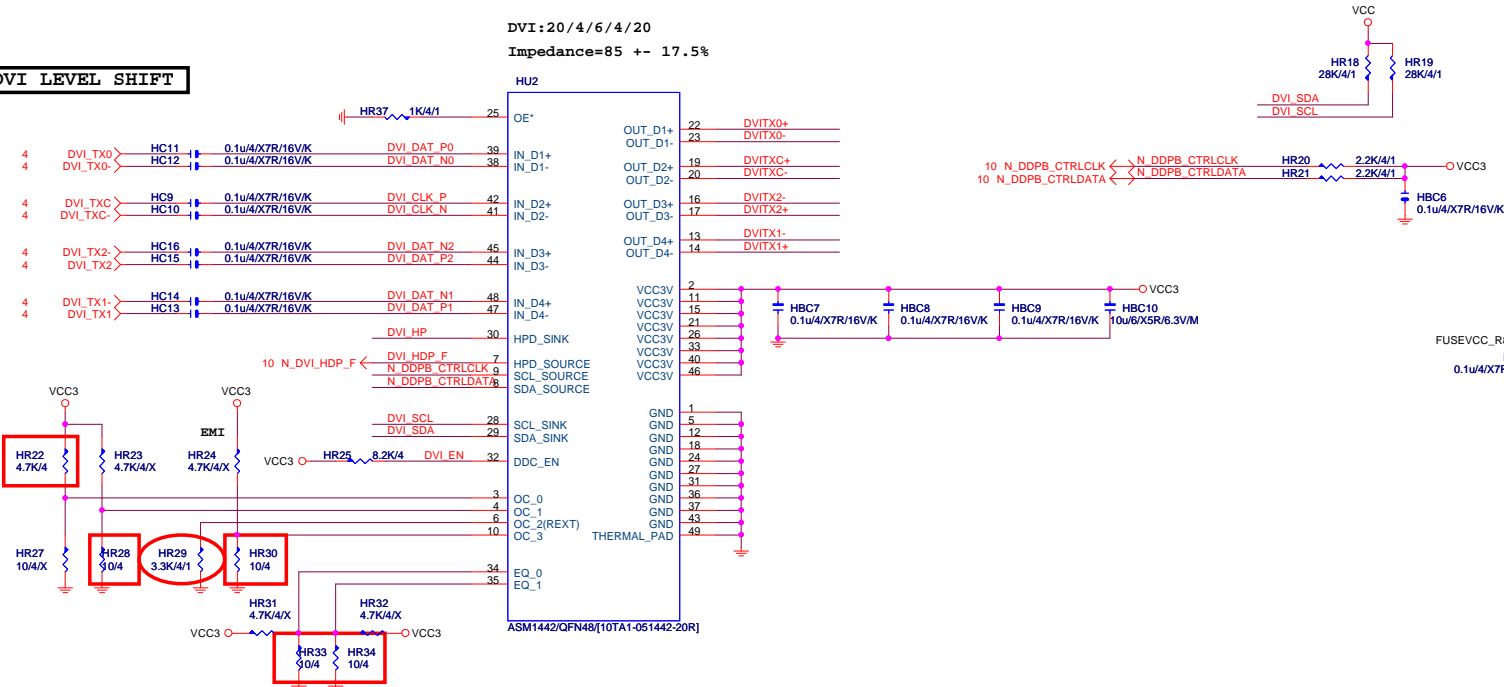


CLOSE USB30 LAN



## DVI LEVEL SHIFT

DVI:20/4/6/4/20  
Impedance=85 +- 17.5%



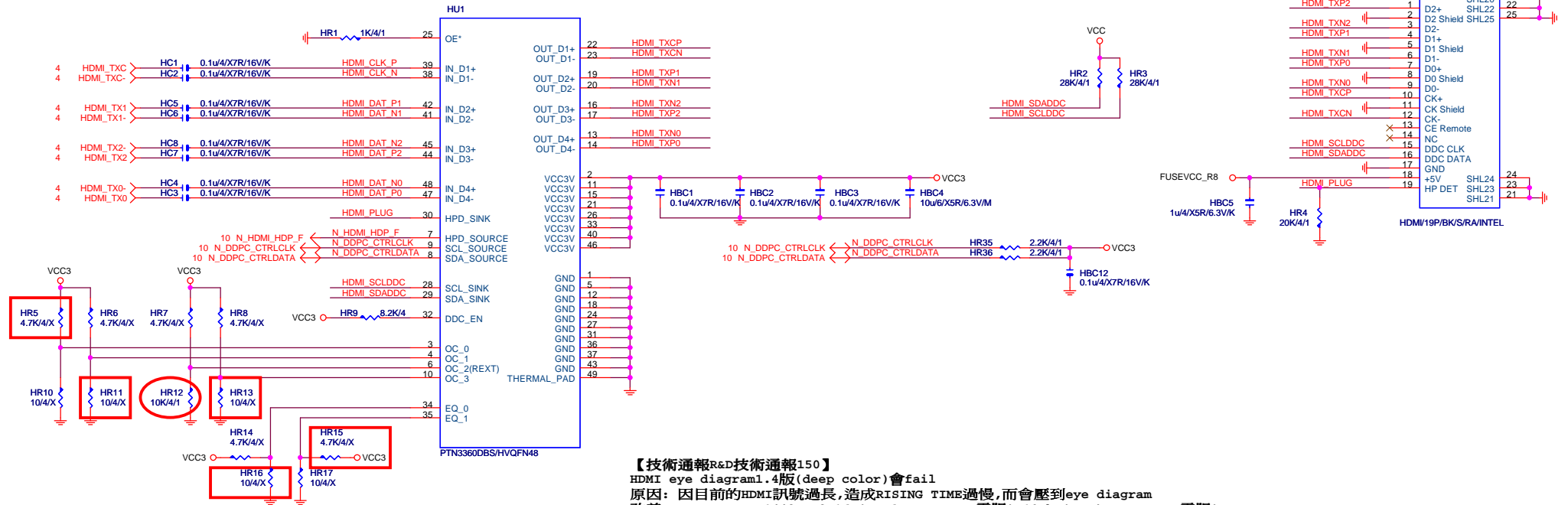
PTN3360:PIN 4/10/34/35 NC PIN,都不上值;只上HR29:10K  
ASM1442:紅色框要上,HR29:3.3K

9:10K  
www.aitech1.ru

<b><i>Gigabyte Technology</i></b>			
Title			
<b>DVI</b>			
Size Custom	Document Number	<b>GA-Z87-HD3</b>	Rev <b>1.02</b>
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# HDMI LEVEL SHIFT

HDMI:20/4/6/4/20  
Impedance=85 +- 17.5%



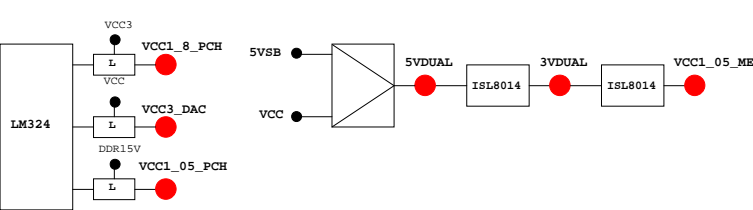
PTN3360: PIN 4/10/34/35 NC PIN, 都不上值; 只上HR12: 10K  
ASM1442: 紅色框要上, HR12: 3.16K

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<b>GIGABYTE™</b>			
Title <b>HDMI</b>			
Size Custom	Document Number <b>GA-Z87-HD3</b>		Rev <b>1.02</b>
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PIN NAME	PWR	AFTER PLUGST	Default	USAGE	NOTE
GP0	MAIN	H-Z	GPI	GPIO0	N/A
GP1/TACH1	MAIN		GPI	GPIO1	N/A
GP2/PIRQE#	MAIN		GPI	-PIRQE	P/U 8.2K VCC3
GP3/PIRQF#	MAIN		GPI	-PIRQF	P/U 8.2K VCC3
GP4/PIRQG#	MAIN		GPI	-PIRQG	P/U 8.2K VCC3
GP5/PIRQH#	MAIN		GPI	-PIRQH	P/U 8.2K VCC3
GP6/TACH2	MAIN		GPI	PCIEX1 Detect	P/U 8.2K VCC3
GP7/TACH3	MAIN		GPI	GPIO7	P/U 8.2K VCC3
GP8	STBY	H	GPI	GPIO8	N/A
GP9/OC5#	STBY		NATIVE	USB OC5#	N/A
GP10/OC6#	STBY		NATIVE	USB OC6#	N/A
GP11/SMBALERT#	STBY		NATIVE	USB PWR protect	P/U 8.2K 3VDUAL
GP12	STBY	L	GPI	GPIO12	N/A
GP13	STBY	L	GPI	LPCPME#	P/U 8.2K 3VDUAL
GP14/OC7#	STBY		NATIVE	USB OC7#	N/A
GP15	STBY	L	GPI	GPIO15(TL8 Enable)	P/U 8.2K 3VDUAL
GP16	MAIN		GPI	GPIO16	P/U 8.2K VCC3
GP17/TACH0	MAIN		GPI	GPIO17	P/U 8.2K VCC3
GP18	MAIN		GPI	Mobile Only	N/A
GP19	MAIN		GPI	GPIO19	P/U 8.2K VCC3
GP20	MAIN		GPI	GPIO20	P/U 8.2K VCC3
GP21	MAIN		GPI	GPIO21	P/U 8.2K VCC3
GP22	MAIN	H-Z	GPI	GPIO22	P/U 8.2K VCC3
GP23	MAIN		GPI	GPIO23	N/A
GP24	STBY	L	GPI	SKTOCC#	N/A
GP25	STBY			Mobile Only	N/A
GP26	STBY			Mobile Only	N/A
GP27	STBY	H	GPO	GPIO27	P/U 8.2K 3VDUAL
GP28	STBY	H	GPO	FWR LED	P/U 8.2K 3VDUAL
GP29	STBY	L	GPI	GPIO29	N/A
GP30	STBY	H-Z	GPI	Mobile Only	N/A
GP31	STBY	H-Z	GPI	Mobile Only	N/A
GP32	MAIN	H	GPO	N/A	N/A
GP33	MAIN	H	GPO	N/A	N/A
GP34	MAIN	H-Z	GPI	-PCI_STOP	P/U 8.2K VCC3
GP35	MAIN	L	GPO	-ACZ_DET	P/U 8.2K VCC3
GP36	MAIN		GPI	N/A	N/A
GP37	MAIN		GPI	N/A	N/A
GP38	MAIN	H-Z	GPI	PCIEX4 Detect	P/U 8.2K VCC3
GP39	MAIN	H-Z	GPI	GPIO39	P/U 8.2K VCC3
GP40	STBY		NATIVE	USB OC1#	N/A
GP41	STBY		NATIVE	USB OC2#	N/A
GP42	STBY		NATIVE	USB OC3#	N/A
GP43	STBY		NATIVE	USB OC4#	N/A
GP44	STBY	L	NATIVE	GPIO44	P/U 8.2K 3VDUAL
GP45	STBY		NATIVE	GPIO45	P/U 8.2K 3VDUAL
GP46	STBY	L	NATIVE	GPIO46	P/U 8.2K 3VDUAL
GP47	STBY			Mobile Only	N/A
GP48	MAIN	H-Z	IN	GPIO48	P/U 8.2K 3VDUAL
GP49	MAIN	H-Z	IN	GPIO49	P/U 8.2K 3VDUAL
GP50	MAIN		NATIVE	-REQ1	P/U 2.2K VCC
GP51	MAIN	H	NATIVE	-GNT1	N/A
GP52	MAIN		NATIVE	-REQ2	P/U 2.2K VCC
GP53	MAIN	H	NATIVE	-GNT2	N/A
GP54	MAIN		NATIVE	-REQ3	P/U 2.2K VCC
GP55	MAIN	H	NATIVE	-GNT3	N/A
GP56	STBY		NATIVE	Mobile Only	N/A
GP57	STBY	H-Z	IN	VCORE_OV1	P/U 8.2K 3VDUAL
GP58	STBY	H-Z	NATIVE	F_USB_OC	P/U 8.2K 3VDUAL
GP59	STBY		NATIVE	USB_OC0#	N/A
GP60	STBY	H-Z	NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL
GP61	STBY	L	NATIVE	-SUSTAT	N/A
GP62	STBY	L	NATIVE	SUSCLK	N/A
GP63	STBY	L	NATIVE	GPIO63	N/A
GP64	MAIN	L	NATIVE	CLKOUTFLEX0	N/A
GP65	MAIN	L	NATIVE	CLKOUTFLEX1	N/A
GP66	MAIN	L	NATIVE	CLKOUTFLEX2	N/A
GP67	MAIN	L	NATIVE	CLKOUTFLEX3	N/A
GP72	STBY	H-Z	NATIVE	VCORE_OV4	P/U 8.2K 3VDUAL
GP73	STBY			Mobile Only	N/A
GP74	STBY	H-Z	NATIVE	1_05V_OV2	P/U 8.2K 3VDUAL
GP75	STBY	H-Z	NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL

PIN NAME	USAGE	NOTE
SVC/PECI_RQT/GP14	-PECI_REQ	
PWROK1/GP13	PWROK1/ITE_PWROK	
KRST#/GP62	-KBRST	
SO/GP50	-ICH_SPI_CS	
IRTX/GP47/CE2_N/JP7	CEB_N	
GP46/IRRX	-LAN2_DSM	
PSION#/GP42	-PSON	
PWROK2#/GP41	PECI_CTL	
PCIRST3#/GP10/VDIMM_STR_EN	-PCIE_RST	
RSMRST#CIRRXX1/GP55	-RSMRST	
PME#/GP54	-LPCPME	
PD5/GP75/BUSS00	N/A	
PIN NAME	USAGE	NOTE
FAN_TAC2/GP52	FANIO2	
FAN_TAC3/GP37	FANIO3	
VIDO3/FAN_TAC4/GP25/DSR2#	FANIO4	
FAN_CTL2/GP51	FANPWM2	
FAN_CTL3/GP36	FANPWM3	
VID4/GP34	BEEP-	
VID3/GP33	TURBO1	
VID2/GP32	TURBO0	
VCORE_GOOD/VID6/GP63	CPUT_LED1_C	
VID5/GP35	CPUT_LED2_C	
VID1/GP31	CPUT_LED3_C	
VID0/GP30	-LAN1_DSM	NBT_LED1_C
SLCT/GP80	CPU_LED1_C	
PE/GP81	CPU_LED2_C	
BUSY/GP82	CPU_LED3_C	
PD3/GP73/BUSSI1	SB_LED1_C	
PD4/GP74/BUSSI2	SB_LED2_C	
VCORE_EN/VID7/GP64	IT_GP64	SB_LED3_C
PD0/GP70	NB_LED1_C	
PD1/GP71	NB_LED2_C	
PD2/GP72/BUSSI0	NB_LED3_C	
GP22/SCK	LOW_PWR_1	
VIDO5/GP27/SIN2	LOW_PWR_2	
PCIRST2#/GP11	-PFMRST1	
PCIRST1#/GP12	-PFMRST2	
3VSBSW#/GP40	CSI_F0	BSEL166_1
SUSCH/GP53	CSI_F1	BSEL166_2
GP23/SI	BSEL166_3/CSISBSL	
VIDO0/GP20/CTS2#	CPUT_LED1_C	BSEL166_4
GP65/VDDA_EN/GB_01	MB_ID2	
PD6/GP76/BUSS01	MB_ID3	
PD7/GP77/BUSS02	MB_ID4	
AFD#/GP86/SMB_C_R	2X PIN	FST_2X8
INIT#/GP85/SMBD_M	SEC_2x8	GTLREF_AD2
ACK#/GP83	DDR_LED1_C	
VIDO1/GP21/DCD2#	DDR_LED2_C	
STB#/GP87/SMBC_M	DDR_LED3_C	
PWRON#GP44	VCORE_OV1	
PANSWH#/GP43	PWRBTSW	
KDAT/GP61	-PWRBTSW	
KCLK/GP60	KDAT	
MDAT/GP57	KCLK	
MACL/GP56	MDAT	
GP66/VLDT_EN/GB_02	NBT_LED1_C	MCLK
SVD/PCIRSTIN#/CIRTX/GP15	PWM2_CR	
KDAT/GP61	PWM2_CR	
GP67/CPU_PG/GB_03	EN_LOADLINE	IT_GP67/-EN_PWM2
SLIN#/GP84/SMBD_R	-EN_PWM2	
PSI_L/FAN_CLT5/CIRRXX2/GP16	-THERM	
VIDO4/GP26/SOUT2	DDR18V_PH2_EN	
VIDO2/FAN_TAC5/GP24/DSR2#	DDR18V_LED	
VIDO6/GP17/RI2#	1_1V_PH_EN	
VIDO7/JP6/DTR2#	JP6	
PD5/GP75/BUSS00	SB_LED3_C	



The diagram illustrates the layout of a CPU socket, showing the connections for various components. The components are arranged around a central CPU SOCKET.

- CPU\_VTT**: A dashed box containing MOSFETs (TQ3, TQ4) and CHOKEs (TL1, DL1).
- VCORE**: A dashed box containing DC and DP regulators (DC\_DQ1, DP\_DQ1, DC\_DQ2, DP\_DQ2, DC\_DQ3, DP\_DQ3) and CHOKEs (DL1, DL2).
- VAXG**: A dashed box containing DC and DP regulators (DC\_DQ1, DP\_DQ1, DC\_DQ2, DP\_DQ2, DC\_DQ3, DP\_DQ3) and CHOKEs (DL1, DL2).
- P-PAK**: A dashed box containing DC and DP regulators (DC\_DQ1, DP\_DQ1, DC\_DQ2, DP\_DQ2, DC\_DQ3, DP\_DQ3) and CHOKEs (DL1, DL2).
- PCH**: A dashed box containing MOSFETs (TQ3, TQ4) and CHOKEs (TL1, DL1).

The diagram also shows the connections for the CPU SOCKET, including the CPU\_VTT, VCORE, VAXG, P-PAK, and PCH components.

線路圖名稱	BIOS選項
Vcore	CPU Vcore
CPU_VTT	CPU Termination
CPU_VAXG	CPU Graphic Core
VCC1_8_PCH	CPU PLL
VCC1_05_PCH	PCH core
3VDUAL	3VDUAL
DDR15V	DRAM voltage
DDRVTT	DRAM Termination
VREF_CA_A/VREF_CA_B	DRAM Address Ref
VREF_DQ_A/VREF_DQ_B	DRAM Data Ref

Z77-D3H :  
PCH :  
12SP2-S05511-01R/02R/03R  
MOSFET :  
12SP2-S08924-01R/02R/03R

	3 pin FAN control	4 pin FAN control	FAN speed	Controller
CPU FAN	FANPWM1	FANPWM3	FANIO1	IT8720
	ICH_FAN_PWM2	ICH_FAN_PWM0	ICH_FAN_TACH0	PCH
SYS FAN	FANPWM2	N/A	FANIO2	IT8720
	ICH_FAN_PWM1	N/A	ICH_FAN_TACH1	PCH
PWR FAN	N/A	N/A	FANIO3	IT8720
			ICH_FAN_TACH2	PCH